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FINAL REPORT

STUDY OF THE DEPOSITION OF SINGLE CRYSTAL SILICON,  
SILICON DIOXIDE AND SILICON NITRIDE ON COLD-SUBSTRATE SILICON

By

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(NASA-CR-188166) STUDY OF THE DEPOSITION OF  
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SILICON NITRIDE ON COLD-SUBSTRATE SILICON  
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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION  
Electronics Research Center  
575 Technology Square  
Cambridge, Massachusetts 02139



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## FORWARD

This report covers the period from 1 May 1968 through 31 October 1969. A review of work accomplished prior to this period is included for completeness. An Interim Report, Study of the Deposition of Single Crystal Silicon, Silicon Dioxide and Silicon Nitride on Cold Substrate Silicon, describes the work during the period from 1 May 1967 to 30 April 1968.

## ABSTRACT

A technique has been developed and a system constructed which permits deposition of thin films on substrates at room temperature. Ions of the material to be deposited are accelerated in a beam toward the substrate; the kinetic energy with which these ions arrive at the substrate is easily controlled and the thermal energy equivalent is of the order of thousands of degrees. Semiconducting, metallic, and insulating films have been deposited.

Among the thin films which have been successfully deposited with this system are the following:

- (a) (111) single crystal silicon films on (111) silicon substrates
- (b) silicon films on insulating glass slides
- (c) molybdenum films on silicon substrates
- (d) insulating carbon films on both silicon and glass substrates

Using this ion beam deposition system thin film capacitors and field effect transistors have been fabricated. The thin film capacitors were made using the insulating carbon films as the insulator and tests have shown an expected resistance to sodium ion diffusion. A resistance to radiation of 1 megarad has also been shown.

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## 1 INTRODUCTION

Research performed earlier in this program prior to the last contract year centered on development of the ion beam deposition system. Films studied were primarily silicon, molybdenum, silicon oxide, and silicon nitride. The deposition and evaluation of silicon films was a major goal of this research. In particular, single crystal silicon films were deposited on single crystal silicon substrates and this was verified by electron reflection diffraction analysis performed by Manlabs, Inc., Cambridge, Mass. Silicon films have also been deposited on insulating substrates. Analysis of the silicon films involved investigation of their rectification characteristics, and measurement of thermal emf's to determine whether N or P type films were deposited. Both P and N type films were deposited on both N and P type substrates and diode characteristics were observed.

The last contract year (1 November 1968 - 31 October 1969) has involved the work described below. The ion beam deposition system developed earlier in this program has been used to deposit a variety of thin films--semiconducting, dielectric, and metallic--and to fabricate thin film devices, notably capacitors and FET's. During the course of this research a number of refinements were made in the deposition system, primarily along the lines of increasing film purity and maximizing the efficiency of the deposition process. The final version of the deposition system is briefly described in this report for the sake of completeness.

The ability of the system to deposit conducting films was investigated. In particular, a number of molybdenum films were deposited on silicon substrates. Also further characterization of silicon films continued.

Investigation of insulating films has also been an area of concern. Among the insulating films investigated in the first contract year were silicon oxide and silicon nitride. In this last contract year highly insulating carbon films were deposited by replacing the silicon ion source electrodes with carbon electrodes. Properties of these carbon films and their utility in thin film device construction are discussed in this report.

To facilitate thin film device construction a multi-electrode ion source was built. This is an ion source with replaceable electrodes. By rotating the appropriate electrode material into place in the gun, any one of the following films may be deposited: silicon, carbon, aluminum, or molybdenum. This ion source as well as the single element ion source were both employed in the fabrication of metal-insulator-semiconductor structures.

The earliest devices built were carbon film capacitors, the evaluation of which included investigating density of surface states between silicon and carbon via capacitance-voltage measurements. Work on fabrication of FET's using insulating carbon as the gate material followed. A description and evaluation of these devices is discussed. Work involved study of metal-semiconductor as well as insulator-semiconductor junctions.

Part of the work reported here was supported with Space Sciences Incorporated funds and with IR&D funds from our parent company, The Whitaker Corporation.

## 2 ION BEAM DEPOSITION SYSTEM

A source of positive ions has been developed for the deposition of thin films. This source can produce positive ions of solid material (such as silicon, metals and insulators) in addition to positive ions of gases. Figure 1 shows the construction of the ion source. There are two vacuum regions (a higher pressure one and a low pressure one) separated by a plasma constriction opening used for differential pumping. The diameter of the constrictor opening is about 1.5 mm. The plasma source chamber is the smaller one where the higher pressure discharge (about  $2 \times 10^{-3}$  to  $50 \times 10^{-3}$  Torr) is used to form the positive ions of materials such as silicon. The discharge in the source chamber is used to introduce the silicon atoms into the plasma where the high energy electrons can ionize them. As is shown in Figure 1, a hollow cavity in a silicon electrode is used as one electrode and a silicon post in the center is used as the other. Positive ion bombardment is able to sputter silicon from the electrode. Thus, solid silicon is used as the source of silicon ions rather than the gaseous  $\text{SiCl}_4$  that was used earlier in this program. There is a considerable improvement in film purity due to the elimination of the Cl gas.

Both electrodes in the deposition source chamber are made of silicon to reduce contamination (for depositing a material other than silicon, the electrode material can be changed to that material if necessary). The ion source can be operated in the glow mode at up to several hundred mA or in the arc mode at a current of several amps. At the higher currents there has been the problem of electrode fracture because of larger electrode heating and the thermal stress of the relatively brittle silicon. Films have been obtained only when the electrodes have been operated in the glow discharge mode. An axial magnetic field is used to modify the electron orbits so that the discharge can operate at lower pressures.

The ions are extracted from the source chamber by means of an auxiliary discharge drawn to a silicon anode located in the deposition chamber. A constrictor fabricated of silicon is used to separate the source

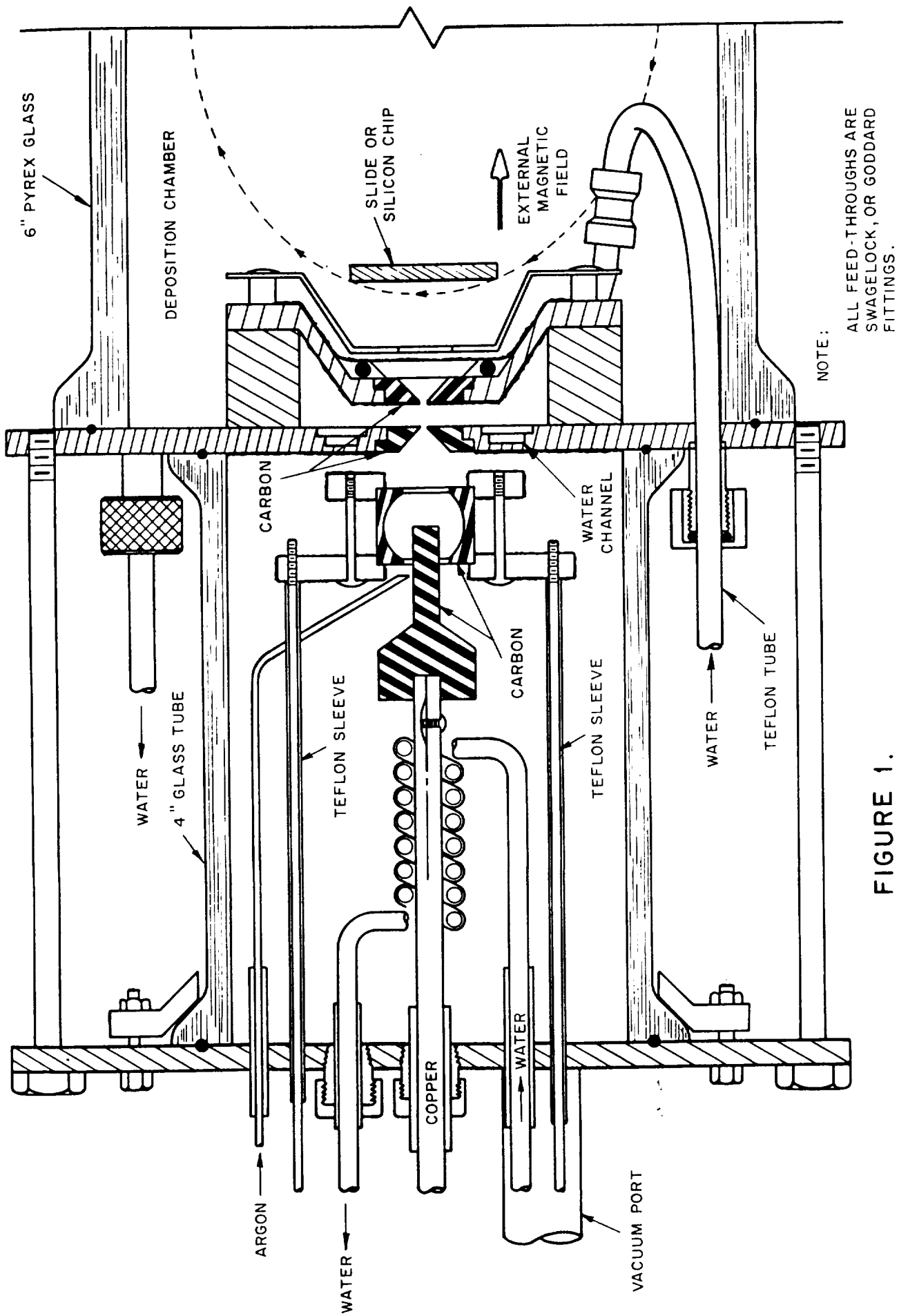


FIGURE 1.  
ILLUSTRATION OF COAXIAL CARBON ARC SOURCE  
FOR PRODUCTION OF CARBON IONS.

chamber and the deposition chamber. The auxiliary discharge is designed so that use is made of the axial magnetic field to orientate the extracted plasma and to reduce the space charge spreading of the beam. By means of the extraction arc, one has a low pressure discharge (in the deposition chamber) in series with the higher pressure arc in the source chamber. Figure 2 shows the associated electrical circuit.

The plasma in the deposition chamber can act as a source of silicon (or other) ions as well as a source of electrons. A negative potential applied to the substrate is used to attract the positive silicon ions. (An unknown fraction of the ion current is due to gas ions but it is assumed to be small.) The ion current is relatively independent of argon pressure in the source chamber.

The ion energy incident upon the substrate can be adjusted by the substrate potential. Before deposition, the substrate is cleaned by sputtering for several minutes at -400 volts; most of the substrate depositions occurred at about -40 volts. The ion current to the substrate is approximately proportional to the extracted arc current. The dependence is shown in Figure 3.

The vacuum system for the deposition system is shown in Figure 4. Differential pumping is used to maintain the deposition pressure in the  $10^{-6}$  range. Figure 5 shows the measurement of the deposition chamber pressure as a function of source chamber pressure. The differential pumping factor is about  $10^{-3}$ .

The purity of the argon gas supply has been increased by modification of the metering and valving system to contain only stainless steel, teflon, and glass. Special drying tubes have been added to remove any possible water vapor. A special trap has been included to remove oxygen from the argon gas feed.

The rotating drum substrate holder has been designed to remove potential impurity sources, and to permit the introduction of a slowly moving nucleating mask, of a variable angle of incidence, of various

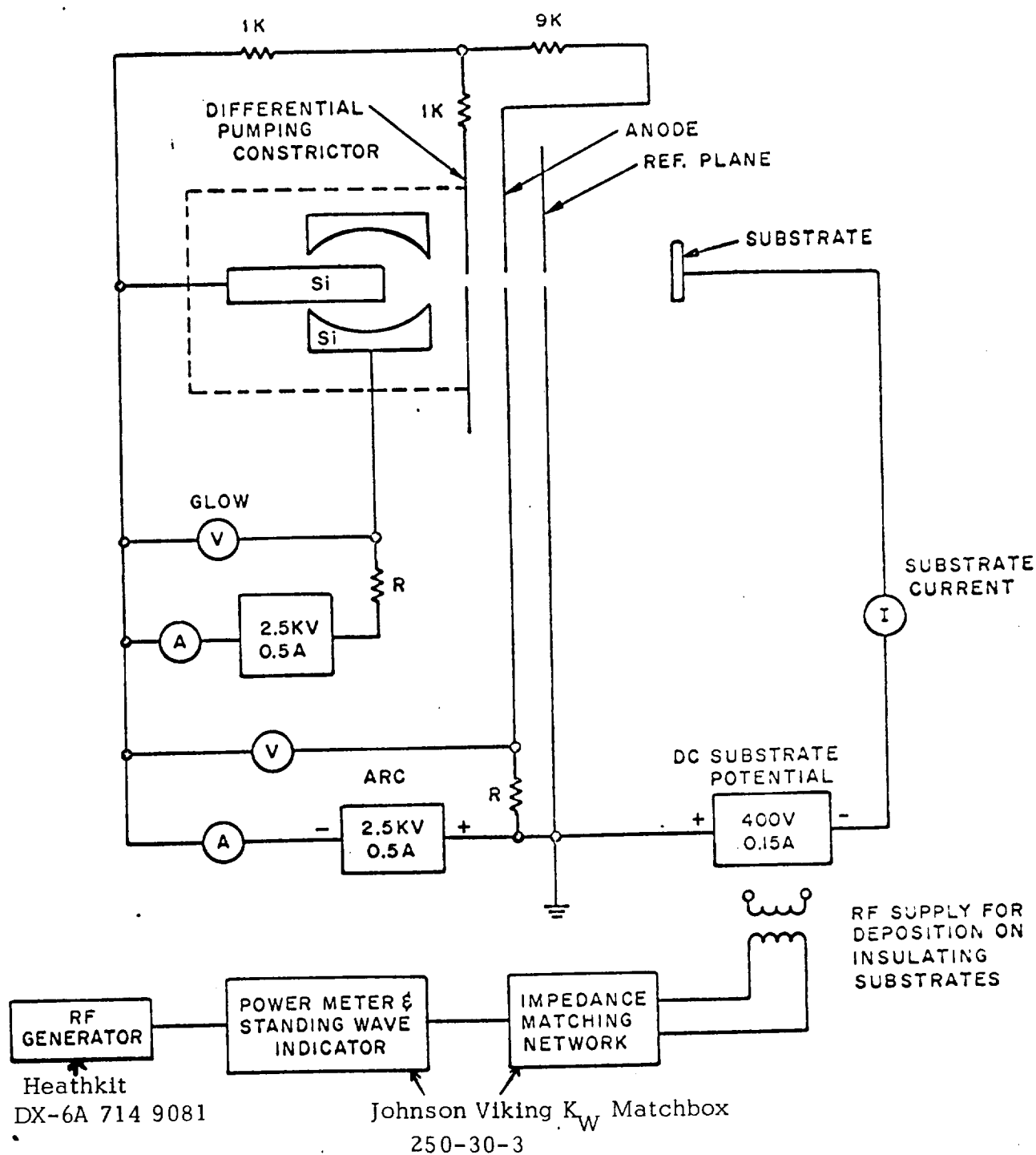


FIGURE 2.  
ELECTRICAL CIRCUIT FOR DC AND RF  
ION DEPOSITION SOURCE.

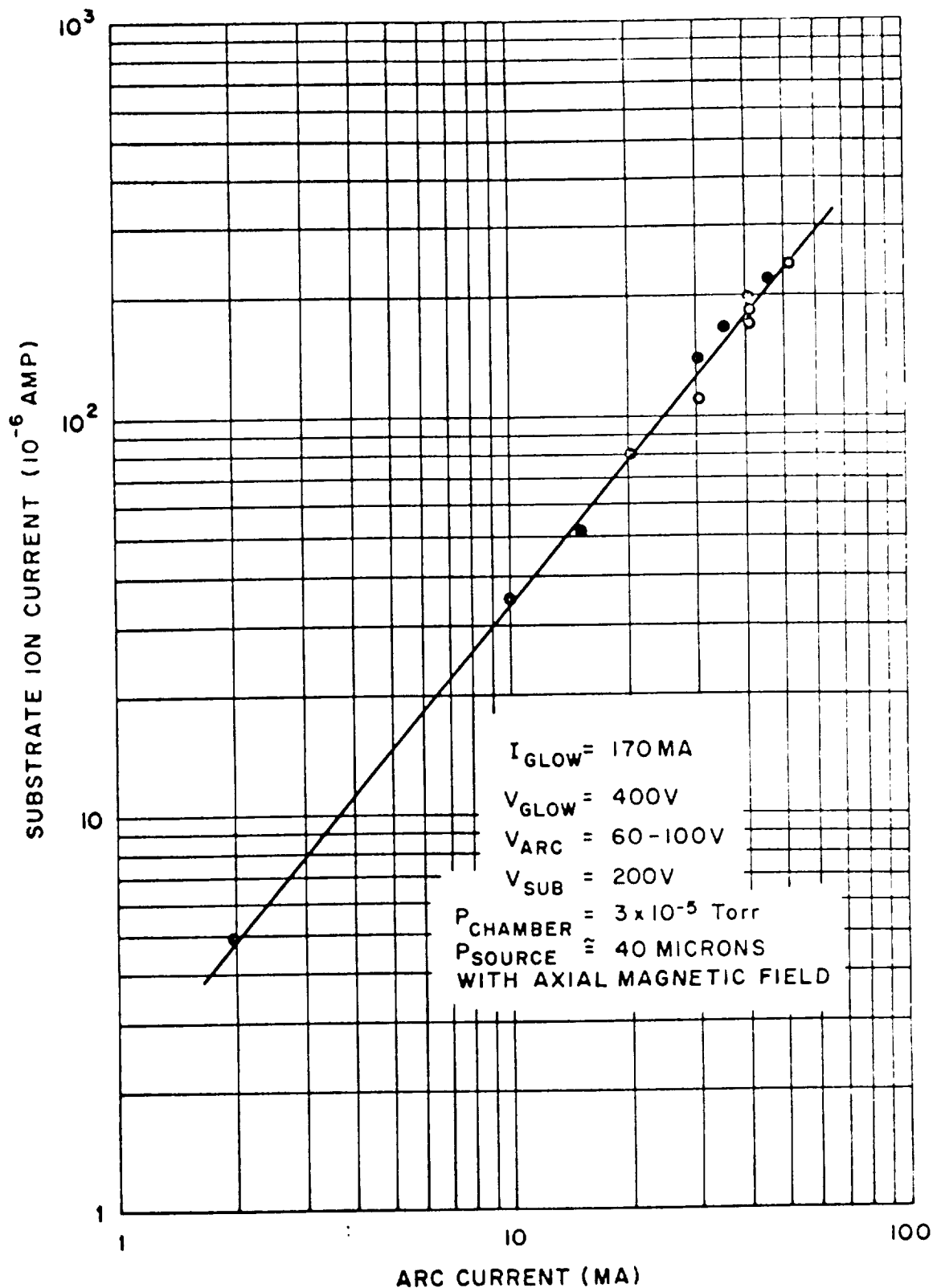


FIGURE 3.

ION CURRENT TO SUBSTRATE AS A FUNCTION OF  
ARC CURRENT  
(FOR SPECIFIC OPERATING CONDITIONS).

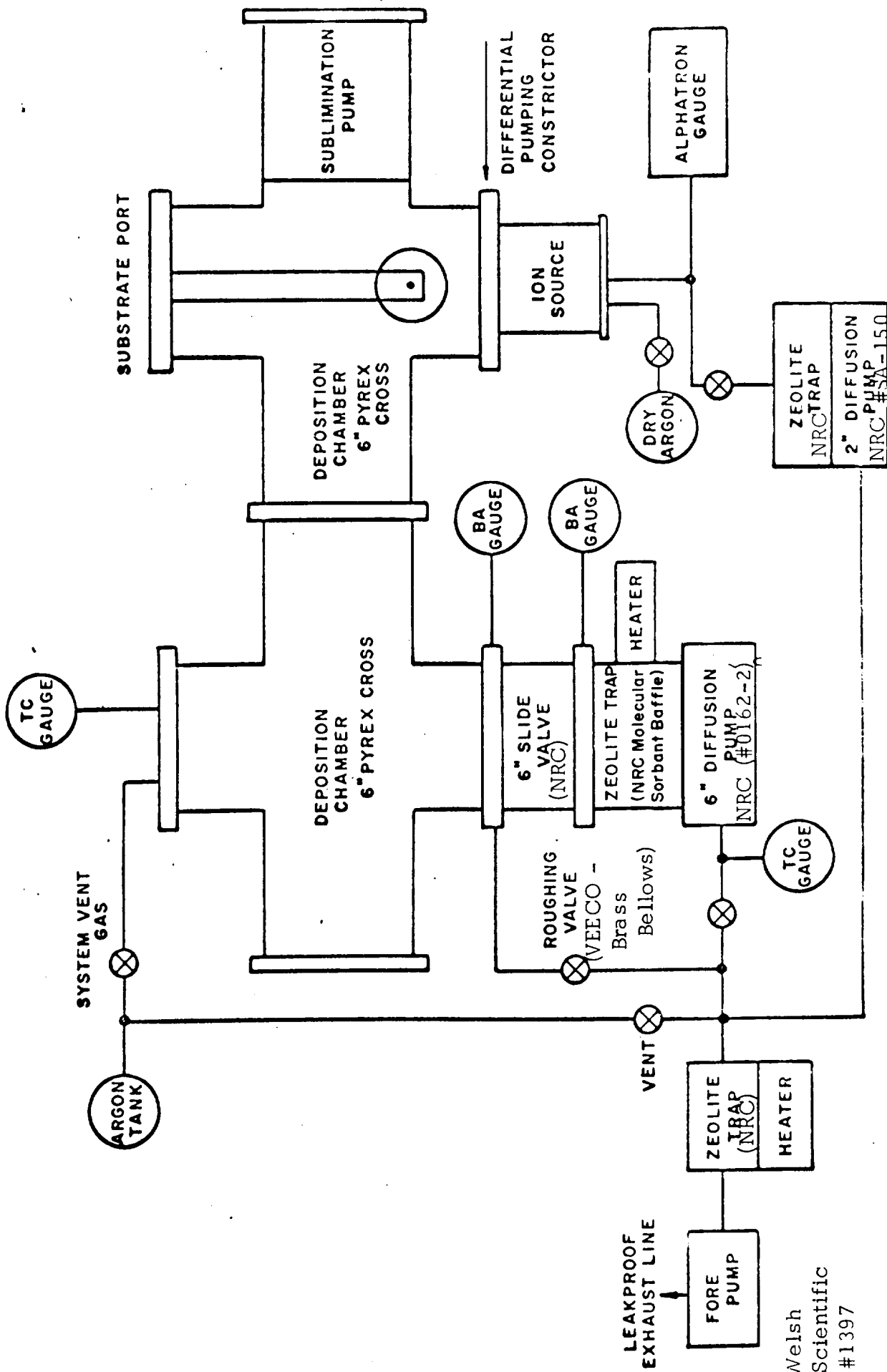


FIGURE 4.  
VACUUM SYSTEM FOR ION BEAM DEPOSITION ON THIN FILMS.

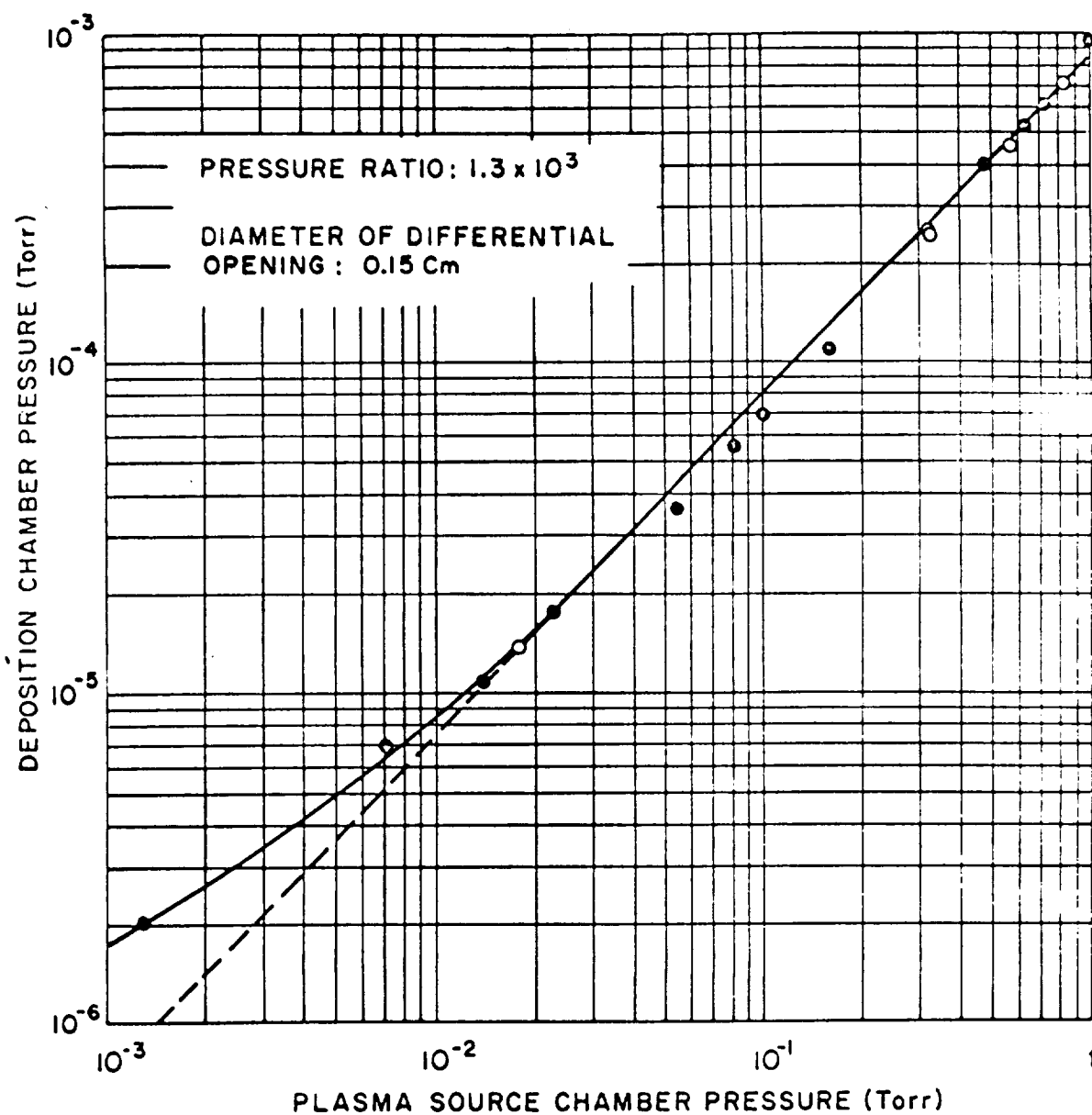


FIGURE 5.  
PRESSURE IN DEPOSITION CHAMBER AS A  
FUNCTION OF ARC CHAMBER PRESSURE -  
FOR SILICON ELECTRODE SOURCE.

potentials on the masks and substrate, as well as controlled and moderate temperature elevation (if necessary) of the substrate to improve outgassing. The moving masks were used sometimes, but were not needed and deposition was predominantly at normal incidence.

The vacuum system includes a titanium evaporation cell in one of the arms of the 6-inch pyrex glass cross. The evaporated films of Ti act as very efficient getters to reduce the chamber vacuum pressure, and particularly that of the troublesome condensable components. The Ti getter films were not used at all times. An additional pyrex glass cross has been included in the vacuum system to bring the number of access ports up from 3 to 5. The vacuum system has been improved to the point where the pressure in the valved-off vacuum system (with the 6 inch valve closed) is about  $1 \times 10^{-8}$  Torr, or better, using the dual zerolite traps and without the need for liquid nitrogen. The vacuum pressure in the deposition chamber (consisting of two of the 6-inch pyrex glass crosses) with the latest plasma arc source mounted is  $2 \times 10^{-6}$  Torr even without the use of the titanium evaporation getter. Thus, it can be concluded that the impurities due to outgassing of the vacuum chamber and the ion source assembly (when cold) have been significantly reduced.

One of the most important features of the silicon source is the use of silicon electrodes to reduce contaminants from other electrode materials. Silicon electrodes are used for the source anode, the source cathode, the constrictor (differential pumping), and for the extraction anode.

When molybdenum or carbon films were to be deposited, the silicon electrodes were replaced with molybdenum or carbon electrodes.

### 3 DEPOSITION OF SILICON FILMS

#### 3.1 Deposition Conditions

Early work in depositing silicon films relied on a gaseous  $\text{SiCl}_4$  ion source. Problems were encountered due to apparent contamination of deposited films by chlorine and oxygen. By converting to high purity solid silicon electrodes as a source of ions and by taking care to remove contaminating oxygen from the system as described earlier, single crystal silicon films were deposited.

A typical rate of growth for these silicon films was about  $10\text{\AA}/\text{sec}$  over a diameter of about 6 millimeters, and film thicknesses of about 0.6 micron or larger were achieved. Both N and P type films were grown on both N and P type single crystal (111) silicon substrates. The deposition conditions for some of these samples is provided in Table 1. Evaluation of these silicon films included tests for etching in hydrofluoric acid, electron reflection and transmission diffraction measurements, thermal emf probe analysis, and investigation of diode characteristics.

#### 3.2 Hydrofluoric Acid Test

Samples showed resistance to etching with HF for periods as long as 20 hours, thus demonstrating that the films are not silicon dioxide or silicon monoxide.

#### 3.3 Electron Diffraction Measurements

The samples listed in Table 1 were sent to Manlabs, Inc., Cambridge, Mass. for electron reflection diffraction analysis. The experimental results for these deposits indicated that all deposits were single crystal silicon with (111) deposit planes. There was no evidence of any portion of the deposits being polycrystalline. By etching away the substrate independent transmission electron diffraction measurements were also made for SSI at Rutgers University. These verified that some of the films have a (111) single crystal structure<sup>16</sup>. Appendix A describes the details of the electron reflection diffraction measurements.

TABLE 1

SUMMARY OF SOME SINGLE CRYSTAL SILICON FILMS ON SILICON  
SUBSTRATES AS DEPOSITED BY THE SILICON ION BEAM SOURCE<sup>(a)</sup>

<u>Sample No.</u>	<u>Substrate Type and Structure</u>	<u>Film Type and Structure</u>	<u>Substrate Potential (volts)</u>	<u>Deposition Time (min)</u>	<u>Deposition Pressure (Torr)</u>
A(#6-12/26/67)	N(111)	P(111)	- 50	10	$1 \times 10^{-6}$
B(#4-12/20/67)	P(111)	P(111)	- 40	5	$2 \times 10^{-5}$
C(#8-12/26/67)	N(111)	P(111)	- 40	5	$1 \times 10^{-6}$
D(#8-12/20/67)	P(111)	P&N(111)	-100	5	$2 \times 10^{-5}$
E(#7-12/20/67)	N(111)	P(111)	-200	5	$2 \times 10^{-5}$

<sup>(a)</sup> Approximate deposition conditions:

Glow current: 50-55 ma at 800-900 volts.

Arc: 50 ma at  $\approx$  200 volts.

Axial magnetic field  $\approx$  1.0K Gauss.

Substrate ion current  $\approx$  200  $\mu$ A.

### 3.4 Thermal Probe Measurements

To help demonstrate the semiconductor nature of the silicon films, the thermal emf generated across the film upon the application of heat was measured. By observing the polarity of this emf, one may deduce whether the deposited film is N type or P type silicon. A heated metal probe used in conjunction with a high impedance voltmeter was first calibrated against films of known doping and then used to investigate the deposited films. Results for a number of samples are tabulated in Table 2. As can be seen, both N and P type films were deposited on N and P type silicon substrates. Since the silicon used in the ion source electrodes was N-type material, one would expect the deposited films to be N-type. However, an excess of crystalline defects tends to result in P-type films, and as shown in Table 2, P-type films have indeed been deposited. It is further expected, however, that the use of higher energy silicon ions in the deposition will lead to a reduction of surface impurities and a higher surface atom mobility. Films formed under high substrate bias, then, should be free from impurities and crystalline defects, and should tend to be N-type. The last entry in Table 2 confirms this: an N-type film resulted for a high substrate bias of -130 v.

An interesting and surprising side result of these measurements was the observation of an unusually high thermal emf of about 10 to 40 volts for some samples. Examples of two such samples are shown in Figures 6 and 7. Sufficient care was employed in making these thermal emf measurements to insure their validity; it is felt that these abnormally high thermal emfs are real and may deserve future investigation; unfortunately, consideration of time and funds under the present contract necessitated the postponement of such investigation.

### 3.5 Rectification Characteristics of Silicon Films

As part of the demonstration that the deposited films are indeed semiconductor rather than insulating (such as  $\text{SiO}_2$  or silicon monoxide), current versus voltage characteristics were measured for films deposited

TABLE 2

THERMAL PROBE DETERMINATION OF SEMICONDUCTOR TYPES  
FOR FILMS DEPOSITED ON SILICON SUBSTRATES

<u>Sample No.</u>	<u>Substrate Type</u>	<u>Film Type</u>	<u>Ion Current (<math>\mu</math>A)</u>	<u>Substrate Voltage (volts)</u>	<u>Deposition Time (min)</u>	<u>Deposition Pressure (Torr)</u>
7-12/26/67	N	P	200	- 40	10	$1.5 \times 10^{-5}$
6-12/26/67	N	P	200	- 50	10	$1.0 \times 10^{-6}$
2- 1/30/68	P	P	200	- 40	14	$1.5 \times 10^{-5}$
5- 1/ 2/68	P	N	200	- 40	14	$2.0 \times 10^{-5}$
4- 1/ 2/68	P	N	200	- 40	14	$2.0 \times 10^{-5}$
7- 2/15/68	P	N	200	-130	5	$2.0 \times 10^{-5}$

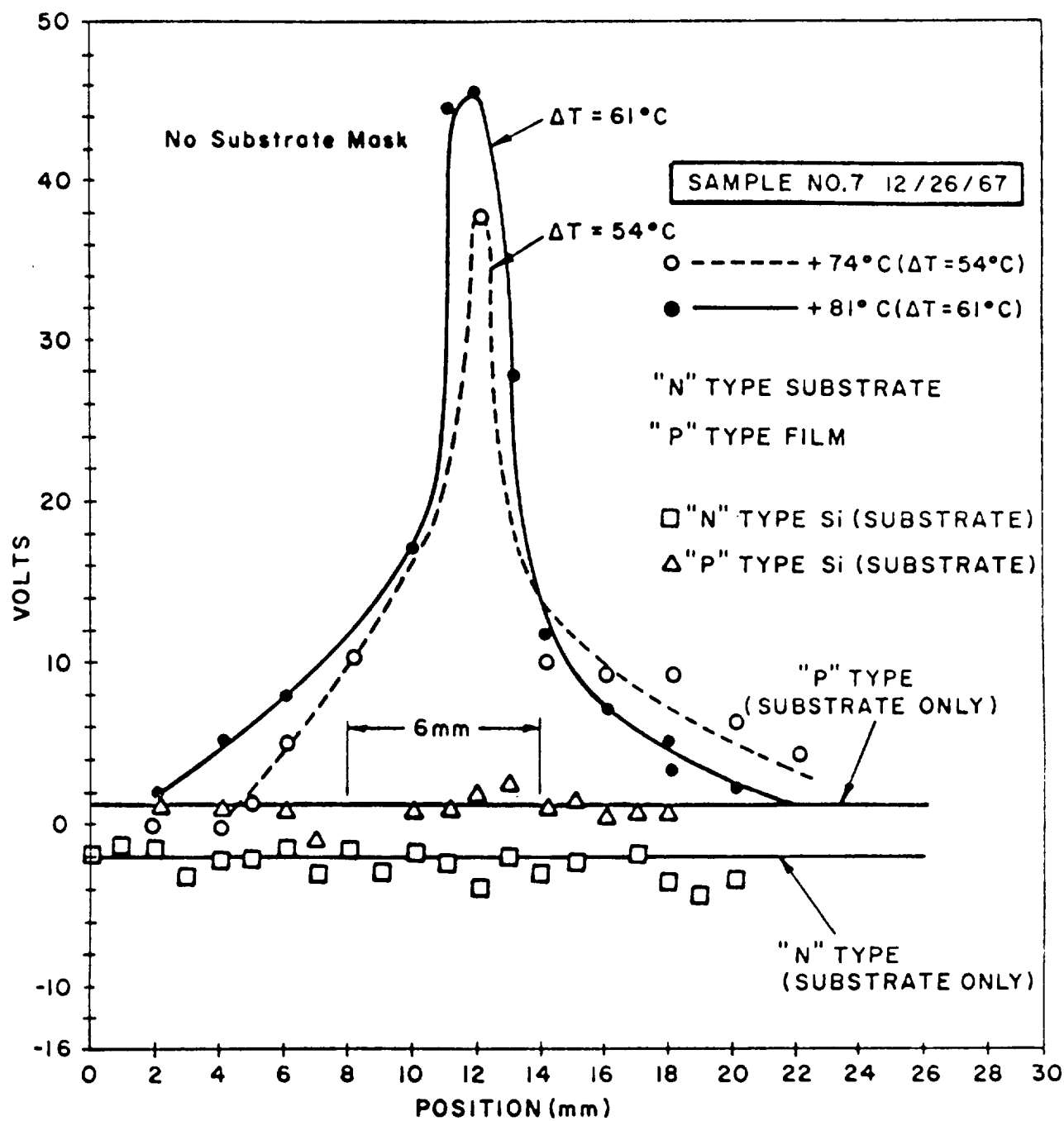


FIGURE 6.

THERMAL EMF DISTRIBUTION FOR  
FILM DEPOSITED ON AN "N" TYPE SUBSTRATE  
-AT TWO DIFFERENT PROBE TEMPERATURES.

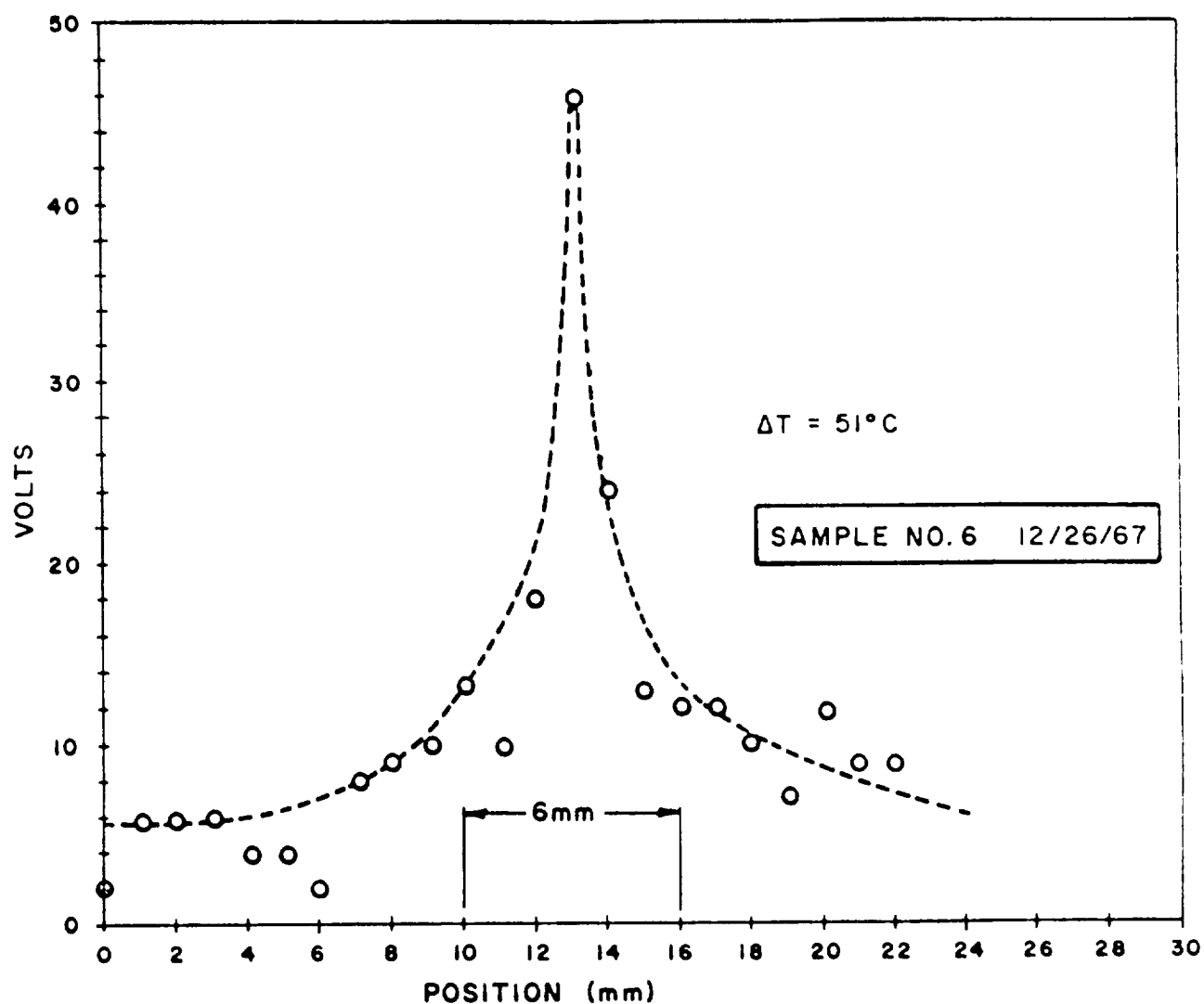


FIGURE 7.

THERMAL EMF PROFILE FOR DEPOSITED FILM  
- SHOWING VERY LARGE DC EMF.

upon silicon substrates. Figure 8 illustrates the results that were obtained. Measurements are shown for the diode characteristics obtained for a portion of the slice that is uncoated with the deposited film. This characteristic serves as a base line "before" characteristic for comparison. The data can be interpreted as representing the case for two metal-silicon diodes connected back to back. Since the forward voltage drop of a diode is small compared to the reverse voltage drop, the reverse diode characteristics of the two diodes essentially predominate. It can be seen from Figure 8 that the saturation reverse diode currents are about  $10^{-7}$  amp. The contact areas of the two metal-silicon junctions are different because the probe diameter is small compared to the substrate diameter. Therefore, it is expected that the reverse current characteristics will not be completely symmetrical.

A measurement was also made of the current versus voltage characteristics for the film deposit on the same substrate. It can be seen from Figure 8 that the characteristics are different because of the film and this can be attributed to the deposition of a different semiconductor film. The expected current voltage characteristic for an insulating film is markedly different from that of a semiconductor. An insulating film would have a much lower current and would be expected to be approximately ohmic. The measured current for the deposited silicon film is greater than that for the substrate (probably because of some lateral current flow in the conducting film) and cannot be ascribed to the presence of an insulating film.

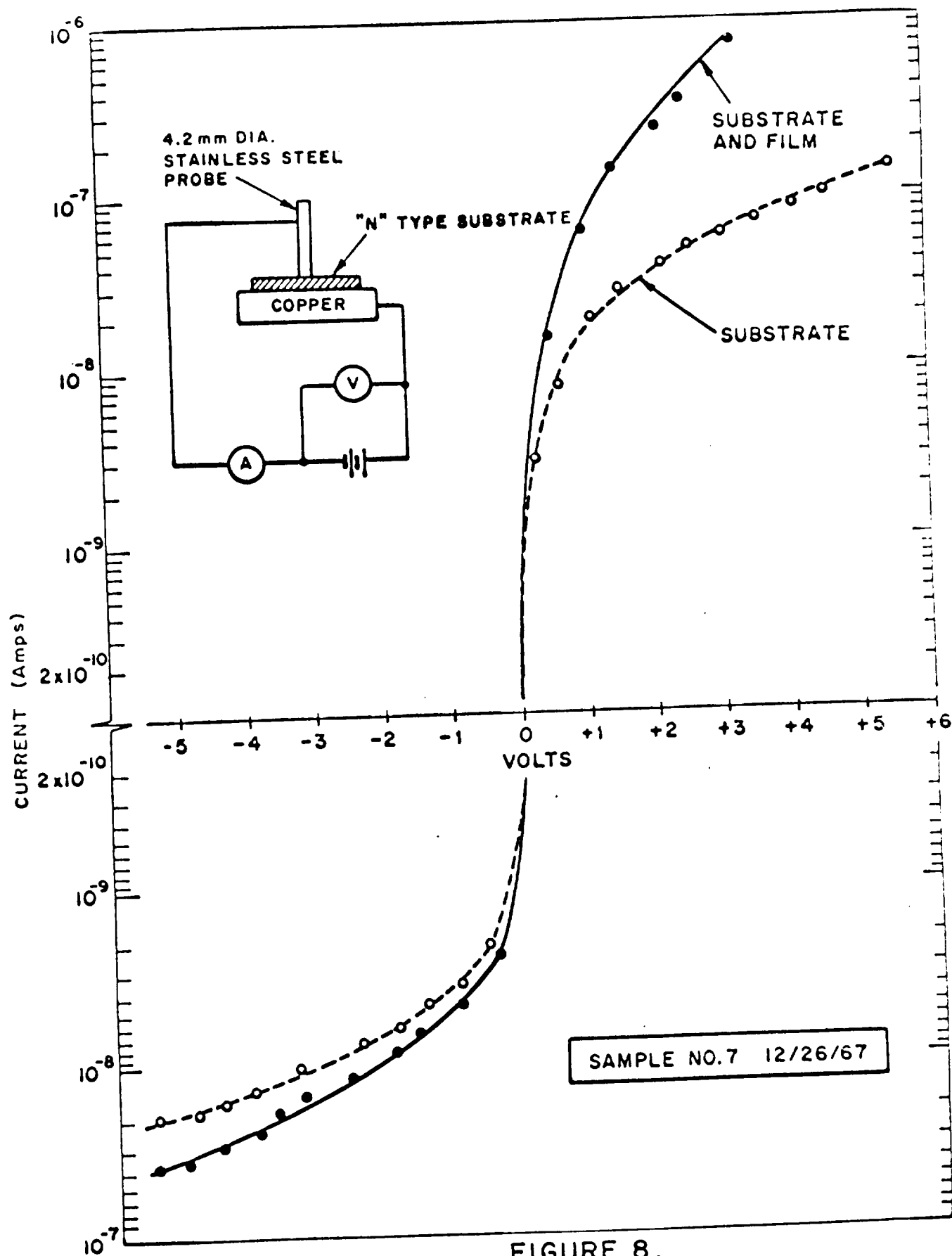


FIGURE 8.  
CURRENT vs. VOLTAGE CHARACTERISTICS FOR  
FILM DEPOSITED ON SILICON SUBSTRATE.

#### 4 RF DEPOSITION OF SILICON FILMS ON INSULATING SURFACES

The ion beam deposition system was also used to deposit silicon films on insulating surfaces; silicon films were formed both on glass slides and on a  $\text{SiO}_2$  film. A difficulty with depositing on insulating substrates is the fact that as positive ions are directed to it, the substrate acquires a net positive charge and the continued arrival of positive ions is retarded. This problem was alleviated by replacing the D.C. substrate bias supply with an R.F. supply. Using the R.F. system it is possible to alternately direct ions and electrons to the substrate with the result of little net accumulation of charge.

## 5 FABRICATION AND EVALUATION OF THIN FILM DEVICES USING THE ION BEAM TECHNIQUE

### 5.1 Technical Approach

During this program time and effort have been devoted to the fabrication of thin film devices using the ion beam deposition technique. The purpose was to demonstrate that devices could be produced using this deposition technique and in particular to show that devices with unusual and desirable characteristics would result from the application of this technique. The amount of effort that was funded for these tasks required that the program concentrate on a number of specific items and tasks. First, it was necessary to develop an insulating film that could be used in conjunction with the silicon film technique that had been developed in the previously sponsored research on thin films. Second, it was necessary to fabricate insulating film structures for evaluation of their suitability as insulators with acceptable leakage currents and satisfactory capacitance versus voltage characteristics. Third, it was necessary to devise the stencil mask structure that would permit the fabrication of field effect transistor devices. Fourth, it was desirable to obtain additional information about the insulating film that was used as the insulator in the field effect transistor device.

There was a fundamental decision to be made in the fabrication of the FET device in terms of the use of thermal oxidation, impurity diffusion, photo-resist masking, and etching techniques. Since a significant advantage of the ion beam deposition technique is that various materials can be deposited with spatial resolution using stencil masks, it was decided that the use of photo-resist masking and thermal diffusion or epitaxial growth would needlessly complicate the process and throw away many of the advantages of the ion beam deposition technique. In other words, it appeared that the best approach was to fabricate the field effect transistor geometry using the ion beam deposition technique, along with the stencil mask, for the deposition of the desired silicon film, the desired metallic contacts, the desired insulating film, and the desired metallic film for the remaining electrodes.

The ion deposition gun was improved so that it consisted of four separate electrodes that could be individually rotated into place so that ion beams of four different materials could be produced and made to impinge on the substrate target. One electrode was silicon, which is used to fabricate the silicon film; the second electrode is carbon, which is used for the insulating film; the third electrode is molybdenum, and the fourth electrode is aluminum. These latter two metallic electrodes are used to give beams of metallic ions for the formation of the conducting film. Since the conducting films can also be produced by thermal evaporation and the ion beam deposition technique offers no significant advantage at present over the use of film evaporation, it was decided to use evaporated metallic films rather than the ion beam deposited metallic films. This was done in the interest of expediency and economy of time and funds. The two difficult tasks are then the deposition of the silicon film on the insulating substrate and the deposition of the insulating film. Since there appear to be no desirable non-thermal methods for producing the silicon and insulating carbon films, these films were specifically deposited using the ion beam deposition sources. These films were deposited using both individual carbon and silicon guns as well as the multi-electrode ion source.

Earlier work had demonstrated that silicon films could be deposited by the ion beam deposition technique. The remaining tasks were to improve the film theory, to characterize the film properties in more detail and to show that usable devices could be fabricated utilizing this ion beam deposited silicon film. In order to short cut the extensive and tedious effort of characterizing the silicon film completely, it was desired to demonstrate initially that satisfactory devices could be fabricated using these films. Once this had been done, then the more detailed evaluation of the properties of the silicon film could be deferred for future work, and effort could be devoted to making the films and devices reproducibly and of increasingly better quality.

It was felt that with the appropriate geometry the question of single crystal size and of grain boundaries in the silicon film would not be of particular concern since either one could design the device so that the current flow would be parallel to the grain boundary or else the grain boundary density within the active region could be reduced by optimization of the deposition parameters.

## 5.2 Insulating Films

A necessary part of the program in the fabrication of FET devices involves the deposition of compatible insulating materials. There was the possibility of thermal oxidation of the silicon film in order to produce the desired insulating layer but it was felt that since the thermal diffusion was not geometrically controllable except through successive photo-resist masking and etching that this is not a technique to be strongly recommended. In addition, it was felt that the silicon dioxide film is not sufficiently immune to impurity diffusion, therefore, would be troubled by trace contaminants such as sodium which have troubled other FET devices. The use of silicon nitride as an insulating film would reduce the difficulty of sodium ion diffusion but would involve a more complicated deposition. The deposition of silicon nitride could occur through sputtering techniques, but it is felt that the development of silicon nitride deposition techniques is a major subprogram in itself. There is also the problem of sputtering through masks. It was decided not to use photo-resist masks but to confine the effort to stencil masks.

One possible way of solving this problem is to use the silicon ion source in an oxygen or a nitrogen atmosphere and to impinge both silicon and oxygen atoms on the substrate or silicon and nitrogen atoms on the substrate so as to develop a film of silicon oxide or silicon nitride. There is a severe problem, however, of control of stoichiometry in terms of both controlling and making reproducible the stoichiometry as well as demonstrating that the stoichiometry is the desired one. This technique of putting down compound insulators can be looked at in future programs.

A much more desirable way of forming the insulator is to avoid the problems of composition ratio and to use insulating carbon film. It was felt that carbon ions incident on a surface would have a significantly high mobility and could move around and nucleate in the diamond structure characteristic of the formation of diamonds under high pressure and high temperature. Carbon in a diamond form is insulating and also because of its very small atomic radius has a lattice structure which would inhibit the diffusion of the relatively larger alkaline impurities such as sodium. In addition, in the insulating carbon film the interatomic spacing in the grain boundary would still be small enough to prevent sodium ion diffusion along the grain boundaries.

Thus, it was felt that the deposition of carbon films using the ion beam deposition source would result in an insulating carbon film with many diamond-like properties.

This was, indeed, found to be the case. Early experiments with the carbon ion source produced films that were transparent and were insulating. Colors were visible in most of these films and these corresponded to optical interference rather than to stain. This was demonstrated by the fact that microscope examination of the film indicated high order interference with sharp fringe contours showing that there were many optical passages through the film in order to build up these interference patterns. This is not possible if the film were an optical absorber. In addition, the brightness of the colors indicated that the index of refraction of the film was significantly different from that of air so that there was an appreciable reflection coefficient at the film air interface. The absence of color due to stain within the film was demonstrated by the disappearance of color when a drop of alcohol or acetone was placed on the carbon film. This shows that the color was not related to impurities within the film. With the alcohol film, the color of the silicon substrate was immediately seen. As the alcohol evaporated, the original interference color returned.

### 5.3 Properties of Insulating Carbon Films

Since the deposition of the first insulating carbon films a good deal of analysis on this type of film has been done. The film appears extremely useful in its own right in that it is an insulator, with a high dielectric constant and a resistance to ionic contamination from external sources--an attractive prospect for the insulating layer in thin film transistors. An additional point of interest is the resemblance to diamond, a resemblance perhaps to be anticipated considering the high energy with which the carbon ions can be deposited. A catalog of observed properties follows.

a) Highly insulating.

Resistance exceeds  $10^{10} \Omega$  (resistivity  $> 10^{11} \Omega\text{-cm}$ )  
(limit of measuring instrument used) Refer to Figure 9  
for resistance profile

b) Able to scratch glass.

This test was conducted twice with the same results. A portion of the film was removed from the substrate and sandwiched between two glass slides which were initially scratch free as ascertained by microscope observation. The film was then ground between the slides and the slides re-examined. Scratches on the glass were observed, often terminating at a piece of the now-mutilated film. Tests on slides without film material added showed an absence of such scratches.

c) Resists hydrofluoric acid.

Soaking for long periods, in some cases as long as 40 hours, did not remove film.

d) High index of refraction.

The carbon film was measured as having an index over 2.0 (using series H index of refraction liquids--set H 1/2<sup>\*</sup>). The index of refraction for diamond is 2.4.

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\* From Scientific Glass Apparatus, Bloomfield, N.J.

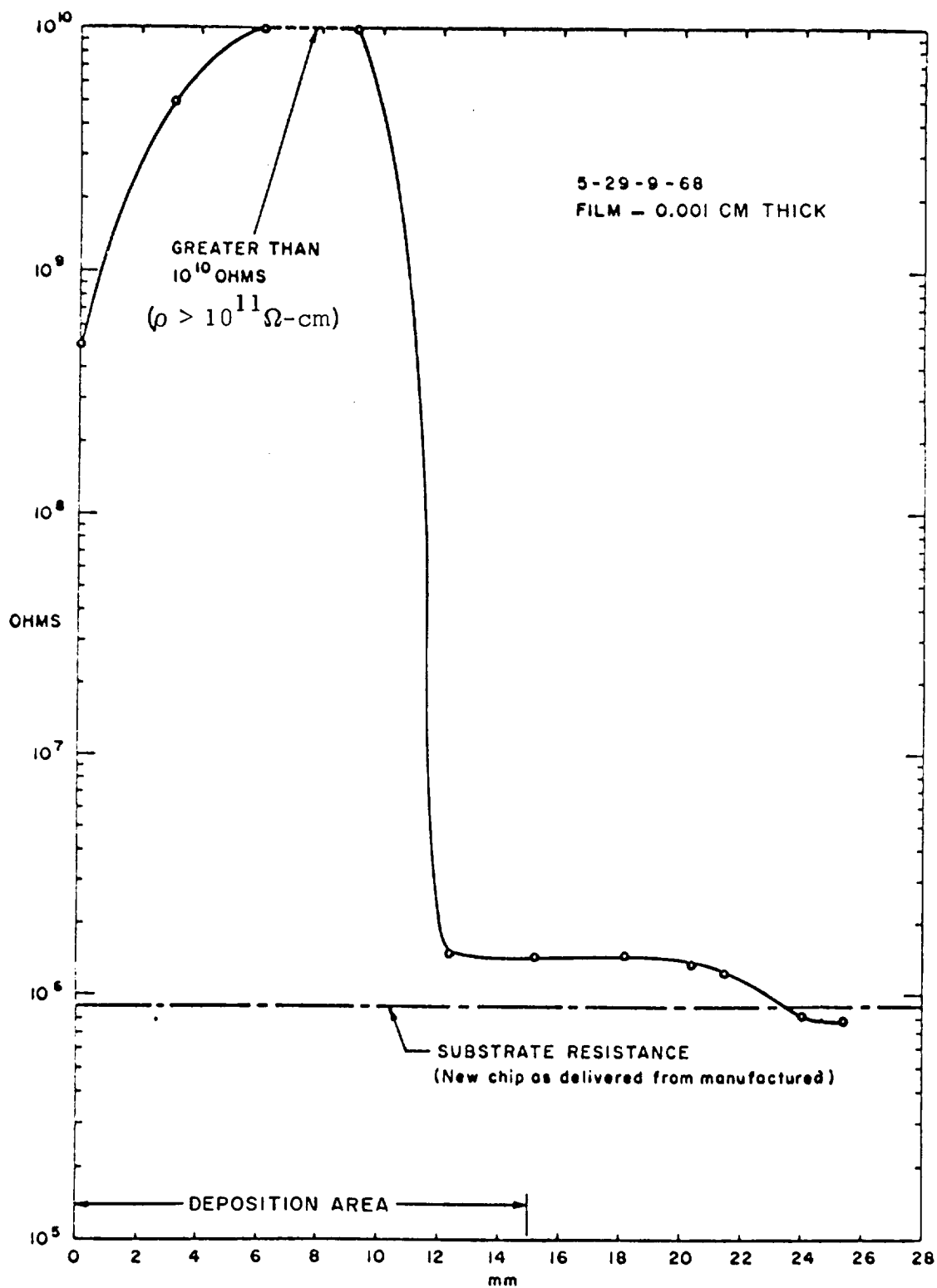


FIGURE 9.  
RESISTANCE PROFILE OF DIAMOND-LIKE CARBON FILM.

e) Transparent.

Pronounced internal fringes were observed.

f) High adhesive force.

The adhesion of the carbon films to silicon substrates was measured and found to be in excess of  $2000 \text{ gm/cm}^2$ .

g) High dielectric constant.

By capacitance measurements the dielectric constant was found to be between 8 and 14. The dielectric constant of diamond is 16.5

h) At least partially crystalline.

X-ray diffraction measurements performed by A. D. Little, Cambridge, Mass. produced ring pattern. Two of the three measured d-spacings are close to those of diamond. These diffraction measurements merit further description.

Several samples of the carbon films were sent to Arthur D. Little, Inc., Cambridge, Massachusetts. These samples are described in Table 3. Transmission and reflection electron diffraction measurements as well as X-ray diffraction by powder camera technique were performed. The X-ray work, performed on Sample C, produced a diffraction pattern of what appeared to be a mixture of two crystalline entities, as indicated by a spot pattern and a ring pattern. The d-spacings for the spot pattern agree reasonably well with the data for silicon and it is, indeed, quite possible that Sample C may have contained small quantities of silicon substrate. The d-spacings for the ring pattern, however, are close enough to those of diamond to be of interest. This data is presented in Table 4. Reference to this table, which also shows handbook data for graphite and copper, indicates that Sample C comes close to copper as well as close to diamond. Considering the materials used in the deposition, it is felt that the presence of copper in the film is highly unlikely. The possibility that silicon carbide has been formed cannot be totally ruled out, but many of the characteristics of the carbon films mentioned earlier do not fit silicon carbide, and it is difficult to explain how the silicon would be continued to be supplied to the top-most layers of deposited carbon as the film thickness increases.

TABLE 3  
CARBON FILM SAMPLES FOR DIFFRACTION ANALYSIS

<u>Sample</u>	<u>Description</u>	<u>Deposition Time</u>	<u>Substrate Voltage</u>
A	Film on 1mm silicon chip	120 mins	80v p-p, 15 KHZ
B	Film on 1mm silicon chip	60 mins	80v p-p, 15 KHZ
C	Capillary tube containing film powder. Sample consisted of film from two independent depositions.	60 mins 55 mins	80v p-p, 15 KHZ plus 60v p-p, 120 KHZ
D <sub>1</sub> and D <sub>2</sub>	Flake of film free from substrate	60 mins	80v p-p, 15 KHZ

Deposition Conditions Common to all Samples:

Arc voltage and current 1.55 kv, 120 ma  
Glow voltage and current -1.6 kv, 20 ma  
Chamber pressure =  $2 \times 10^{-6}$  Torr

TABLE 4  
TABLE OF D-SPACINGS  
(Data compiled by Arthur D. Little Inc., Cambridge, Mass.)

<u>Ring or Spot</u>	<u>Sample C</u>		<u>Silicon 5-0565**</u>	<u>Diamond 6-0675</u>	<u>Graphite 12-212</u>
1	3.15A*	Spot	3.138A		3.37A
2	2.10	Ring		2.06A	
3	1.90	Spot	1.920		
4	1.89	Ring			
5	1.64	Spot	1.638		1.68
6	1.28	Ring		1.26 1.08	1.23

\* The second decimal is a very rough estimate

\*\* ASTM Reference Number

The electron diffraction work was done on Samples D1 and D2. No diffraction pattern was obtained, indicating that these particular films seem to be amorphous. Reflection diffraction measurements, done on Sample B, produced a pattern characteristic of the silicon substrate; apparently the incident electron beam with its extremely small angle of incidence was "looking at" the silicon edge of the 1mm silicon substrate on which the carbon film was grown.

It seems possible to draw the following conclusions from this diffraction work. The carbon film has not been completely characterized; but the X-ray powder pattern measurements, when considered in the light of other of the film properties--high index of refraction, high dielectric constant, ability to scratch glass, resistance to sodium ion diffusion--all these together strongly point to the existence of a diamond structure. The fact that no crystallinity was observed in the transmission diffraction work may have been the result of peculiarities in the specific sample tested, or it may be that the ion beam deposition system is capable of depositing both amorphous and crystalline carbon films. Regardless of the exact identification of the film, it has been possible to fabricate thin film devices using this carbon film as an insulator. Capacitors and FET's have been built and are discussed in the sections that follow.

#### 5.4 Carbon Thin Film Capacitors

5.4.1. Introduction--As part of the program to study insulating films and to investigate the dielectric-single crystal silicon interface, and in preparation for FET fabrication, a number of metal-insulator-semiconductor structures, namely, capacitors, were made using insulating carbon as the dielectric. Measurements of capacitance versus voltage, of current versus voltage, of voltage breakdown, of density of surface states, and of resistance to sodium ion diffusion at elevated temperatures were made. Part of this work was performed with the assistance of Dr. E. Apgar of NASA Electronics Research Center, Cambridge, Massachusetts. Results in brief were as follows:

1) capacitances measured typically around 20 pf ( 0.02 pf/mil<sup>2</sup>) and showed a theoretically predicted voltage dependence, 2) leakage currents were in some cases very low; a number of devices demonstrated diode characteristics, apparently due to the existence of a diode junction at the carbon-silicon interface, 3) voltage breakdown varied from 7 v to 40 v depending on device quality, 4) surface state density is of the order of  $10^{11}$  cm<sup>-2</sup>, and 5) a resistance to sodium ion diffusion was observed. A sketch of the multiple capacitor configuration used in this work is provided in Fig. 10.

5.4.2 Capacitance--For each device made, the capacitance consists of essentially two components, namely the bulk capacitance of the insulating carbon layer plus any space charge capacitance associated with the carbon-silicon interface. Since no depletion region exists when no voltage is applied to the device, measurements at zero bias give the bulk capacitance of the carbon layer alone.\* Capacitance measurements were made on a Fluke 710A Impedance Bridge at 1kHz and zero bias and were verified with a Tektronix 130 L-C meter operating at 140 kHz; these results are tabulated below for nine capacitors.

<u>Substrate Number</u>	<u>Substrate Type</u>	<u>Capacitor Number</u>	<u>Capacitance</u>
1	N (1 $\frac{1}{2}$ -cm)	1	26.2 pf
		2	23.5 pf
		8	10.2 pf
		11	17.8 pf
2	P (1 $\frac{1}{2}$ -cm)	1	34.0 pf
		2	25.0 pf
		3	31.0 pf
		4	20.0 pf
3	P (1 $\frac{1}{2}$ -cm)	1	18.0 pf

A theoretical check on the reasonableness of these results is immediately possible by applying the equation for the capacitance of a parallel plate

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\* In reality, the existence of charges within the carbon layer plus the effect of metal semiconductor work function differences can shift the capacitance-voltage characteristic so that the capacitance at zero voltage is not strictly the bulk capacitance.<sup>3</sup> This effect was examined and is considered later in this report. For the present, however, this effect may be neglected.

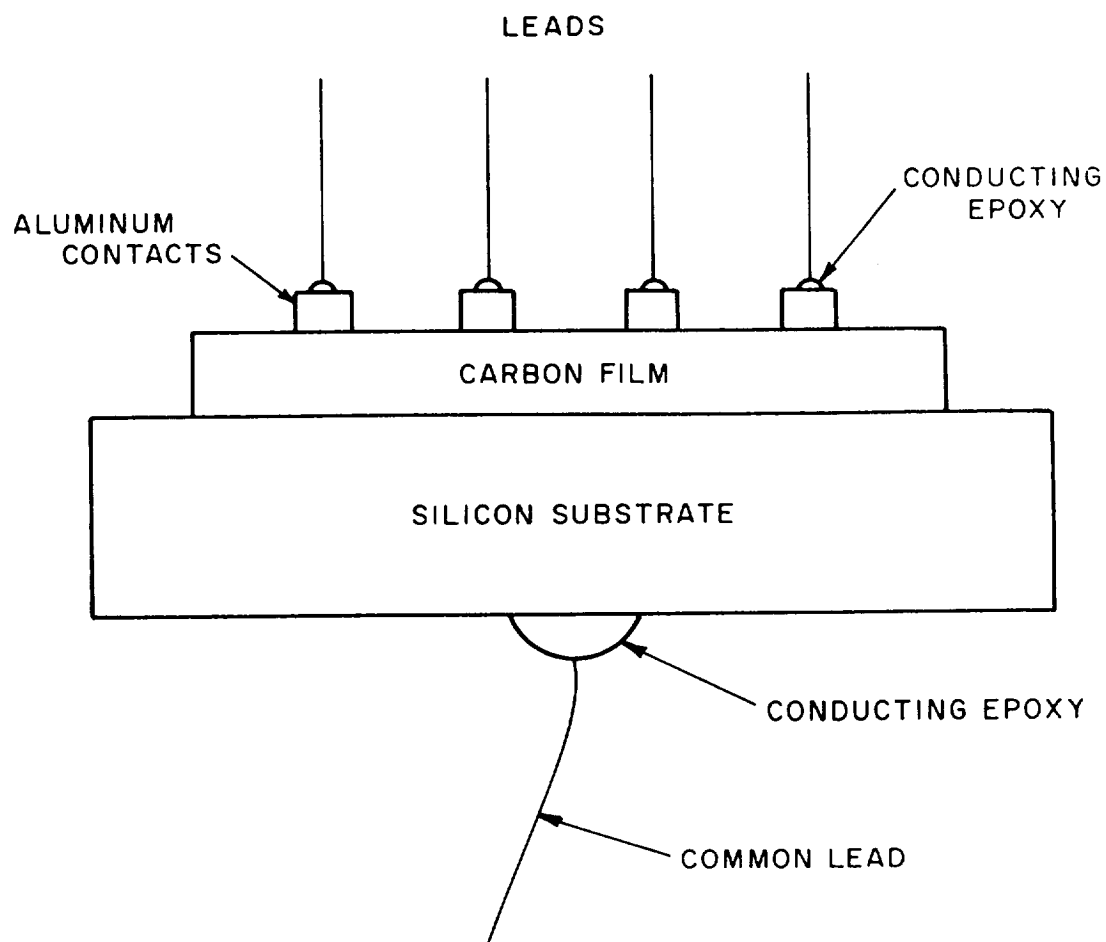


FIGURE 10  
MULTIPLE CAPACITOR CONFIGURATION.

capacitor

$$C_c = \frac{k\epsilon_0 A}{L} \quad (1)$$

where,

$C_c$  = bulk capacitance of carbon film,

$k$  = dielectric constant of diamond-like carbon film = 17  
(Value for diamond<sup>9</sup>),

$\epsilon_0$  =  $8.85 \times 10^{-12}$  farad/meter,

$A$  = area of plate =  $8 \times 10^{-7} \text{ m}^2 \pm 30\%$ , and

$L$  = film thickness =  $3 \mu \pm 50\%$ .

Substituting these values gives  $C_c = 39.6 \pm 58\%$  which, within the accuracy of the calculation agrees generally with the measured values.

The following should be noted:

- (1) The value used for  $k$  is that for diamond, namely 17. Agreement between empirical and theoretical results for  $C_c$  when this value of  $k$  is used in the calculation, is further evidence of the diamond-like nature of the carbon film.
- (2) The large uncertainty associated with the area  $A$  is partially accounted for by the uncertainty involved in evaporating aluminum contacts of exactly 1 mm diameter. An additional uncertainty involves the fact that the surface of the carbon film is not perfectly flat, thus the effective area of the capacitor is not exactly  $\pi r^2$ .
- (3) The measurement of film thickness,  $L$ , by fringe counting techniques involves a large uncertainty. (Optical thickness versus physical thickness.)
- (4) To insure that there was no contribution to the measured capacitance from the substrate itself and from the contacts to that substrate, the following was done. A bare silicon substrate was cleaned in hydrofluoric acid and leads attached in a manner similar to that described for the capacitors. A negligibly small capacitance was measured for this configuration, thus supporting the validity of the previous measurements.

Later in this program a number of capacitance measurements were also performed by Dr. E. Apgar of NASA ERC. Two carbon film samples were supplied

by SSI and the appropriate aluminization was performed at NASA; a thickness measurement of some of these films was also made using a Sloan Angstrometer. Reproductions of the photographs resulting from these thickness measurements are shown in Appendix B. Typical thicknesses were found to be about 500 Å and capacitance values were generally about 30 pf. When this information was used to calculate the dielectric constant,  $k$ , of these carbon film samples, values of  $k \approx 1-2$  resulted. This contrasts sharply with previously measured values, which within the uncertainties mentioned in (2) and (3) above, appear to be between 8 and 14. The only apparent explanation for this is a possible inconsistency in the carbon film from sample to sample. Supporting this explanation is the fact that films measured at SSI and films measured at NASA were not necessarily deposited under identical conditions; that is, no effort was made to measure similar films from a single deposition "batch" at both locations. It should also be recalled that previously mentioned x-ray and electron diffraction work had revealed that both amorphous and crystalline carbon films had been deposited in the past. This is further evidence that there may be radical differences in film samples. Finally, in some of Dr. Apgar's later work in measuring capacitance-voltage characteristics of similar structures, there was noted a considerable difference in film quality not only from sample to sample, but in some cases even amongst capacitors fabricated in different areas on the same film sample. All this points to the fact that the deposition of high quality carbon films is not an easily repeatable task and further optimization of deposition conditions might be worthwhile.

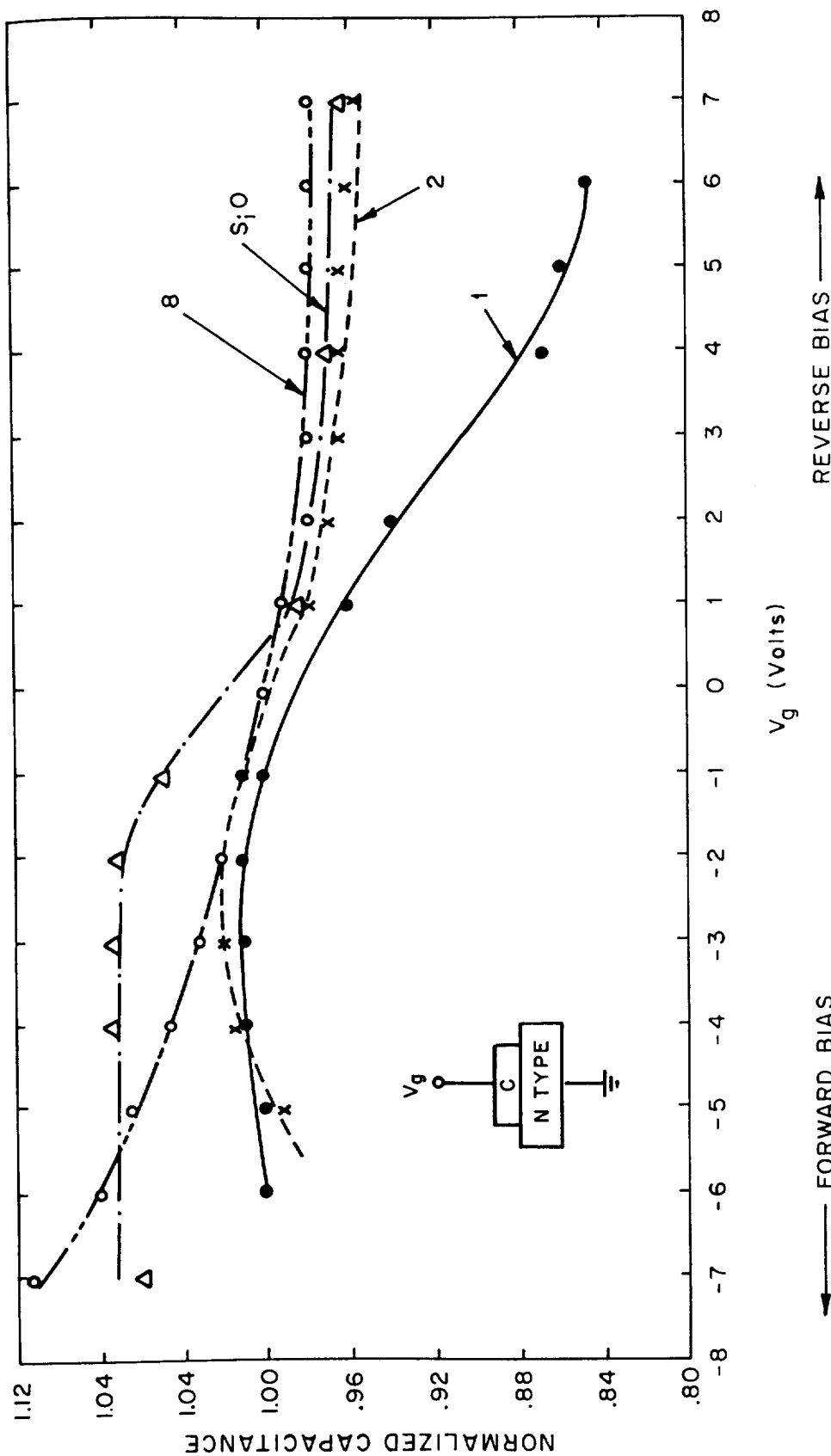
5.4.3 Capacitance as a Function of Voltage--Capacitance-voltage measurements were made on several of the capacitors that were fabricated. This is a standard technique used often in evaluating metal-insulator-semiconductor structures and is discussed in more detail in Appendix C. In general, the measurements were consistent with the theory presented in Appendix C, that is to say curves plotted showed the effect of a depletion layer capacitance in series with the bulk carbon capacitance and showed a predicted voltage dependency.

Figure 11 includes the capacitance-voltage characteristics of four capacitors fabricated on an N-type substrate. For reference purposes, measurements on a silicon dioxide film capacitor are also included. As can be seen, the general shape of the curves shown resembles that predicted by the theory. That is, for large values of reverse bias voltage, the capacitance tends to level off, indicating that maximum depletion width has been reached. For forward bias there is no depletion layer and the capacitance again generally levels off, this time at a value characteristic of the bulk carbon capacitance. The transition from forward to reverse bias is marked by the expected decrease in capacitance.

Several points of interest should be noted in regard to Figure 11. First of all, the voltage dependency of the capacitance is not extremely strong. This essentially says that the thickness of the carbon film ( $\sim 2$  microns) is so great as to tend to swamp out the effects of the voltage dependent depletion layer capacitance. For illustration purposes, Figure 12 presents a graphic illustration of the published effect of increasing insulator thickness on the capacitance-voltage characteristics for a silicon dioxide film<sup>3</sup>. The published results for a  $1\mu$  thick silicon dioxide film are similar to the results obtained for the carbon film.

Second, there is apparent a slight shift in the entire capacitance-voltage characteristic. That is to say, maximum voltage is reached at a slightly negative  $V_g$  rather than at zero volts. As mentioned earlier this may be caused by differences in metal-semiconductor work functions and/or by the existence of surface states at the insulator. Predominance of the latter effect is suspected as will become clear when the results of additional tests are described later in this report.

A number of additional capacitance-voltage measurements were performed by Dr. E. Apgar at NASA ERC, Cambridge, Mass. This data is shown in Figs. 13 through 17. Film thickness for these devices were considerably smaller than those discussed earlier ( $\sim 500 \text{ \AA}$  as compared to  $1-2\mu$ ), and as would be expected for such devices, a stronger voltage dependence



CHIP NO.1  
CAPS 1,2,8, & 11

CAP. NO.	C @ OV	DIA.
1	26.2 pf	1mm
2	23.5 pf	1mm
8	10.2 pf	1mm
11*	17.8 pf	1/16"
$SiO$	142 pf	

\* Curve not shown, but almost duplicates curve 1

FIGURE 11.  
NORMALIZED CAPACITANCE vs. VOLTAGE.

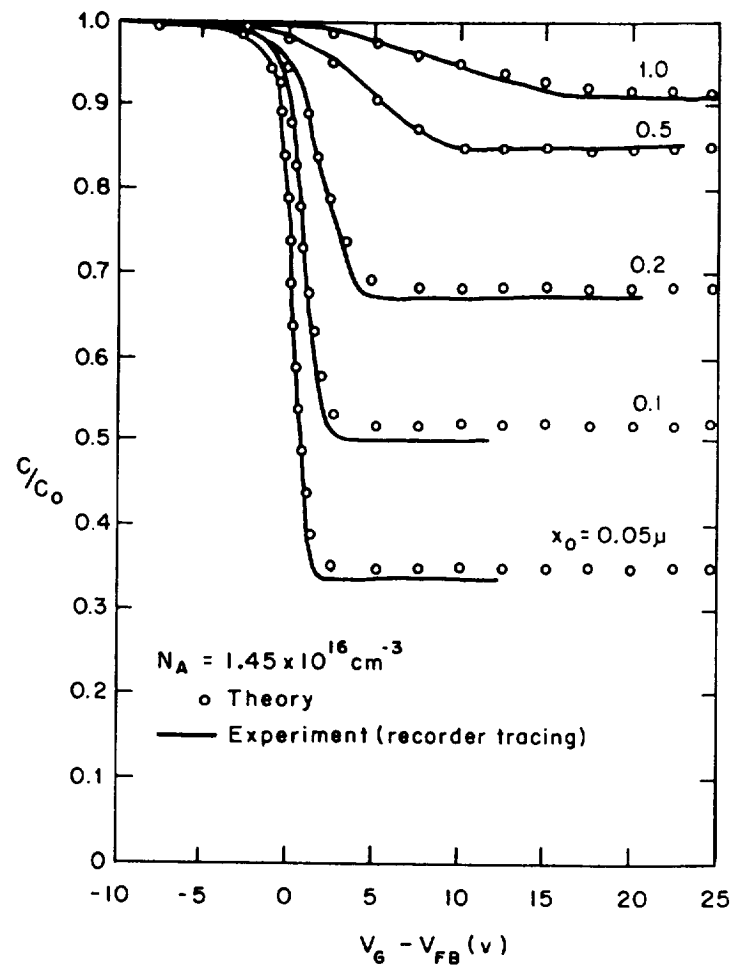


FIGURE 12  
The Effect of Oxide Thickness On  
The C-V Characteristics of MOS Structures\*

\* From Grove, Physics and Technology of Semiconductor Devices(Ref. 3)

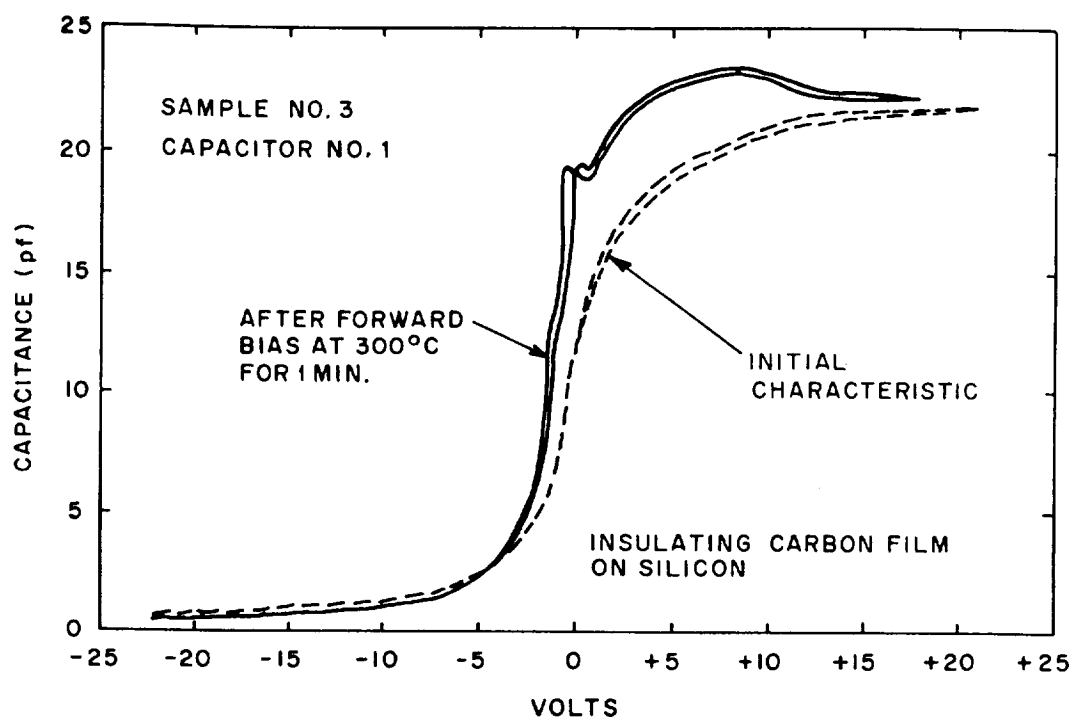


FIGURE 13.  
CAPACITANCE AS A FUNCTION OF  
APPLIED VOLTAGE.

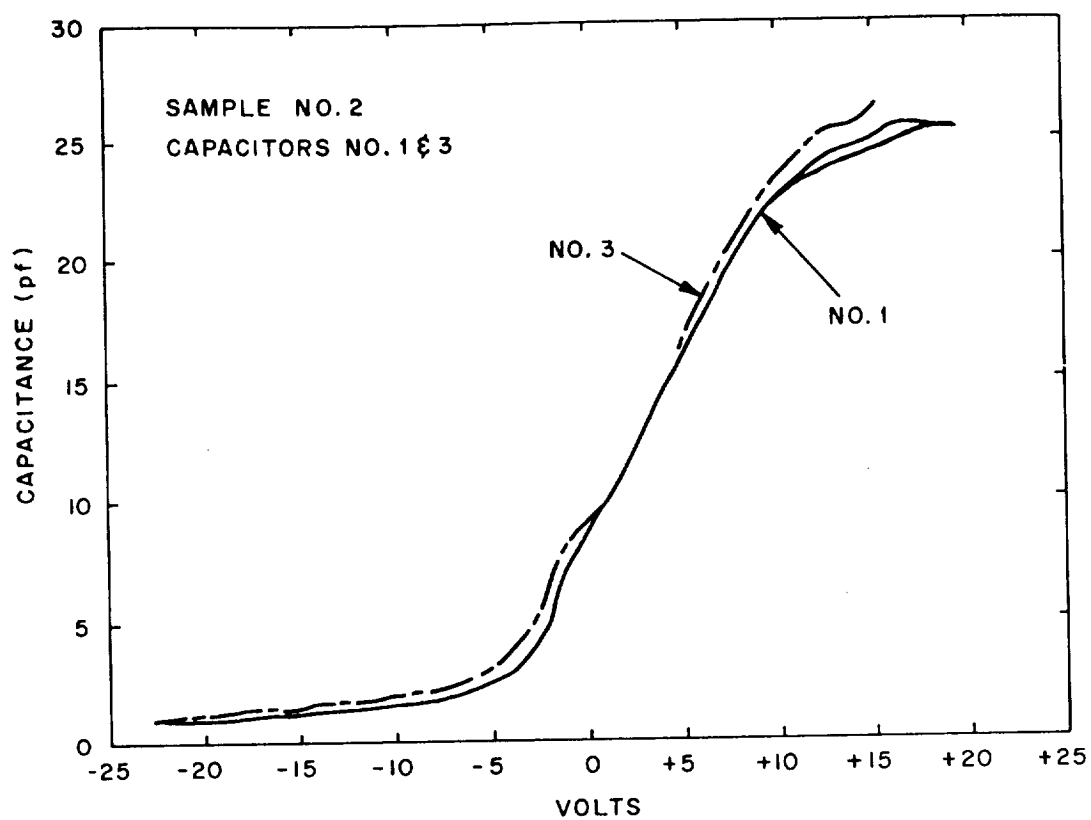


FIGURE 14  
CAPACITANCE AS A FUNCTION OF  
APPLIED VOLTAGE.

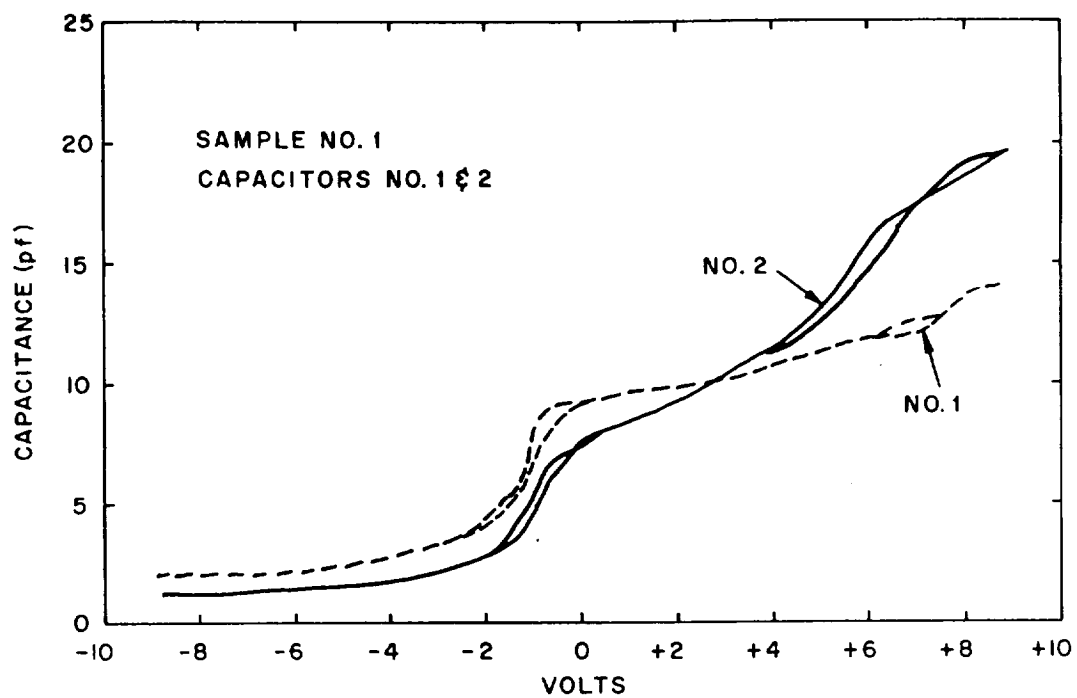


FIGURE 15  
CAPACITANCE AS A FUNCTION OF  
APPLIED VOLTAGE.

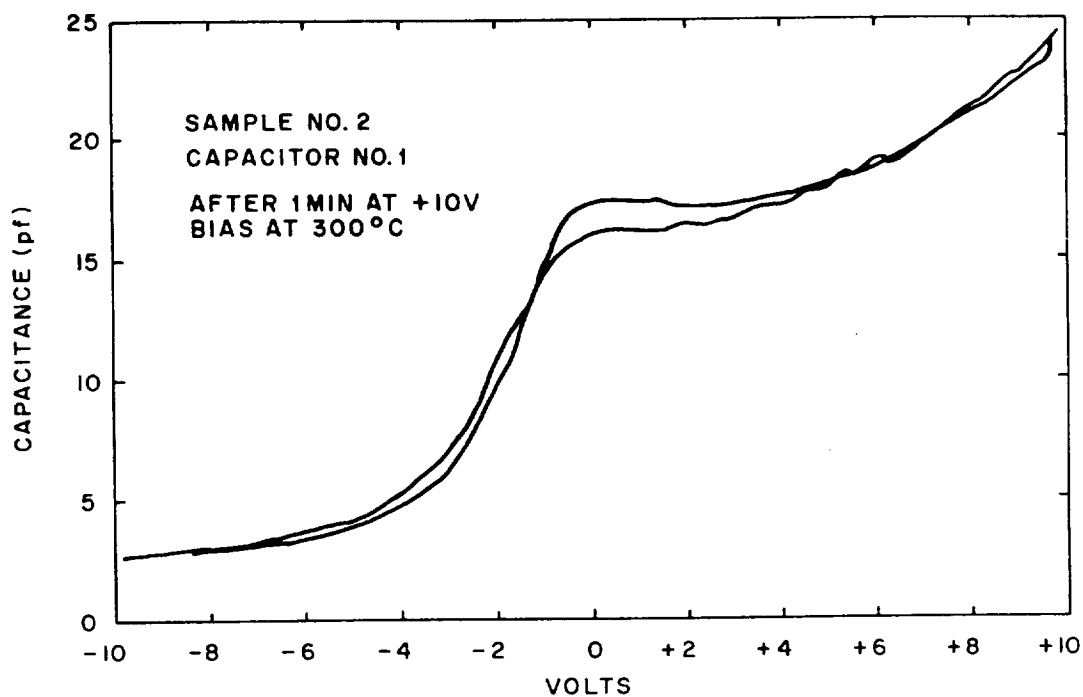


FIGURE 16  
CAPACITANCE AS A FUNCTION OF  
APPLIED VOLTAGE.

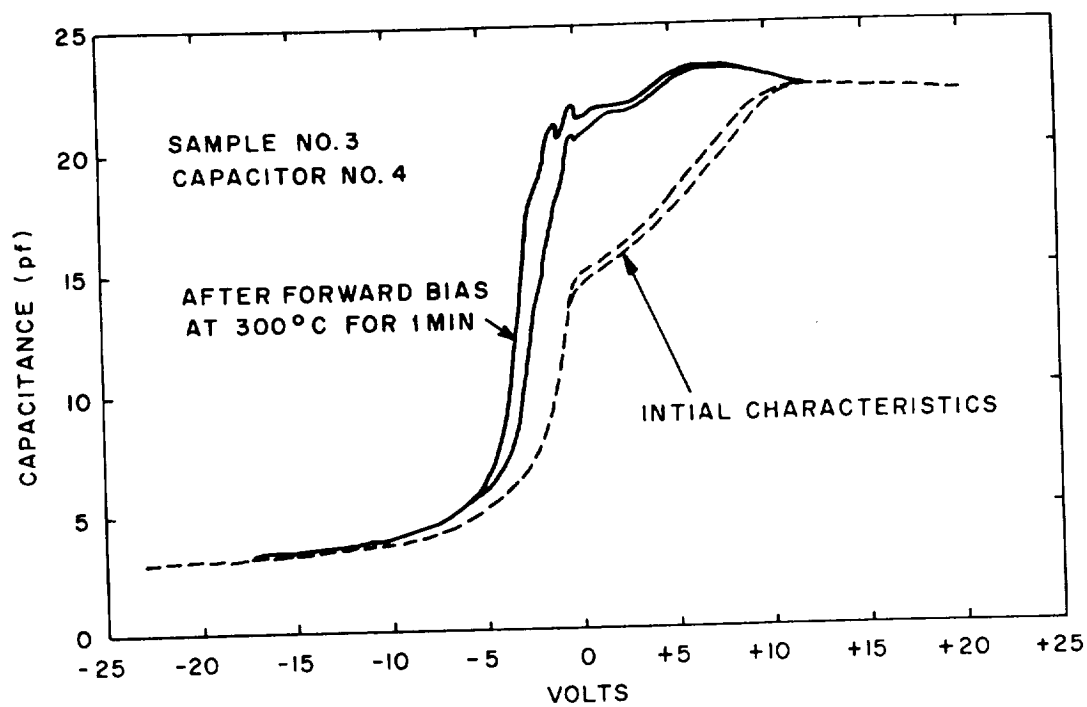


FIGURE 17.  
CAPACITANCE AS A FUNCTION OF  
APPLIED VOLTAGE.

is apparent. Also, as before, there is a shift in the flat band voltage away from zero. If this shift is attributed to the existence of surface states, it is possible to calculate the density of surface states from Eq. (2) below<sup>15</sup>

$$N_{ss} = \frac{C_c \Delta V}{A q} \quad (2)$$

where

$N_{ss}$  = effective density of surface states for insulator-semiconductor interface

$C_c$  = bulk carbon capacitance  $\approx 30$  pf

$A$  = area of capacitor  $\approx 2 \times 10^{-3} \text{ cm}^2$

$q$  =  $1.6 \times 10^{-19}$  coul

$\Delta V$  = shift in flat-band voltage  $\approx 5$  v (e.g. from Fig. 13)

This calculation results in the very reasonable value of about  $5 \times 10^{11} \text{ cm}^{-2}$ .

There is another characteristic of these C-V plots that may be further evidence of the existence of surface states, namely the "kinks" apparent for instance, in Figs. 13, and 17. If surface states are present they behave as a parallel capacitance  $C_{ss}$ ; and  $C_{ss}$  is a voltage variable element which has a maximum for some specific gate voltage<sup>11</sup>. If the surface states have well-defined levels, the total capacitance of the device may show one or more maxima as the voltage is increased. This, indeed, seems to occur for several of the devices tested.

5.4.4 Current versus Voltage--Capacitors fabricated on both N and P type silicon substrates were checked for leakage current for both polarities of each device. It was found for a number of capacitors that a diode junction existed at the carbon-silicon interface, and in many cases the characteristics of this diode dominated the current-voltage characteristics. In other cases capacitors were made which showed no diode properties and which had relatively low leakage currents in both directions.

The curves shown in Figs. 18, 19 and 20 demonstrate the diode nature of the current-voltage characteristics for several capacitors. Two

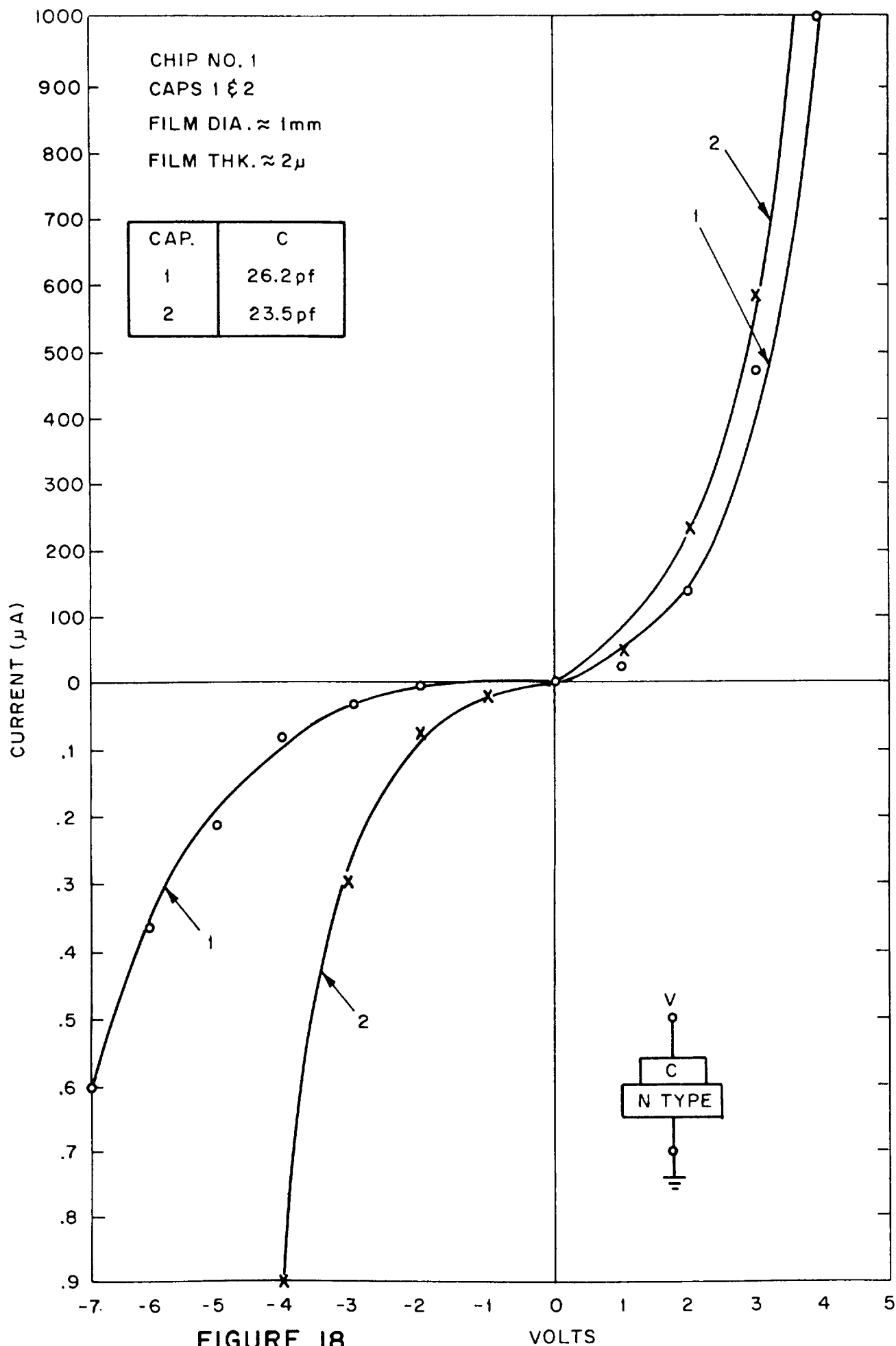


FIGURE 18.  
CURRENT- VOLTAGE CHARACTERISTICS.

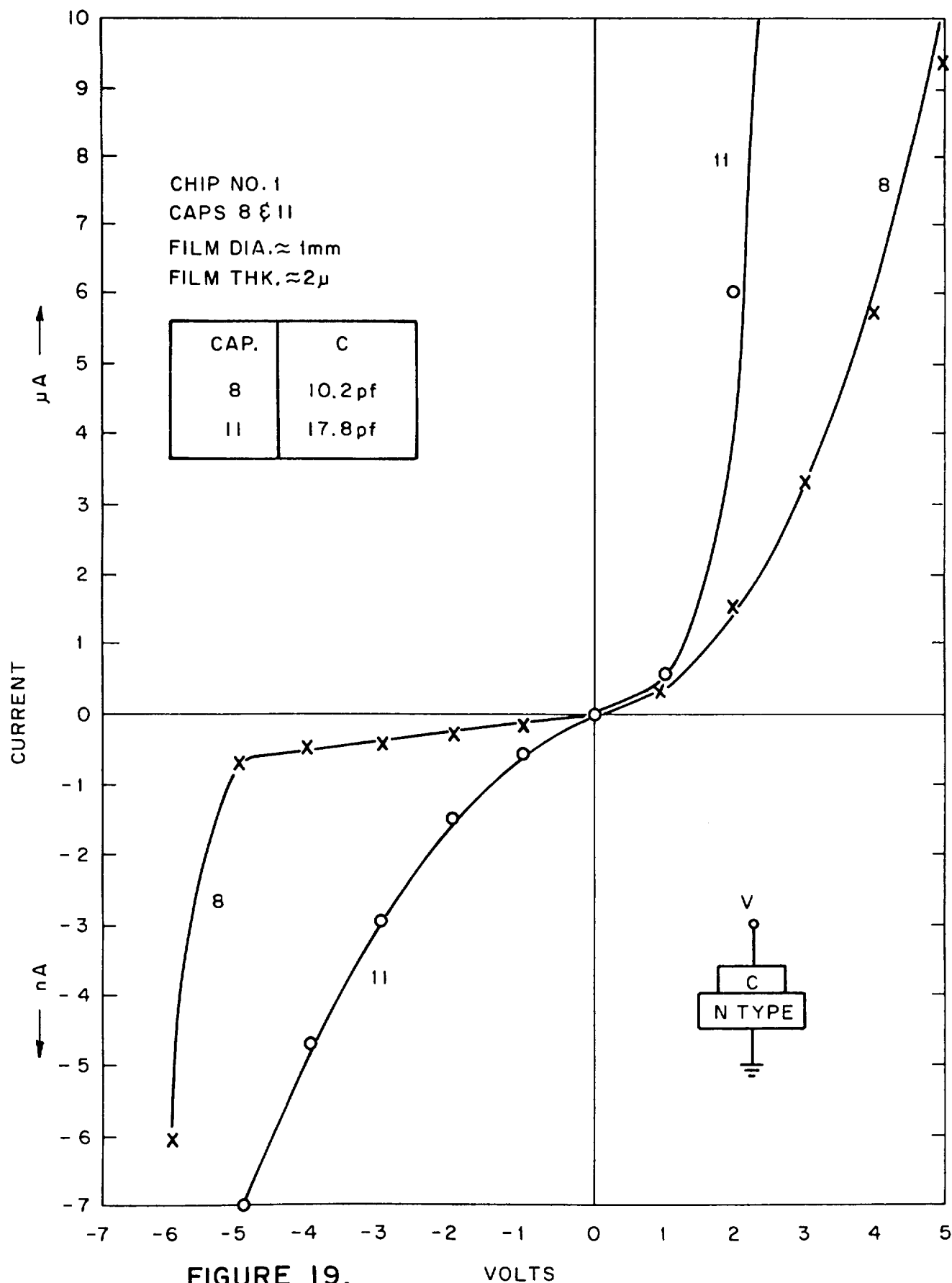


FIGURE 19.  
CURRENT-VOLTAGE CHARACTERISTICS.

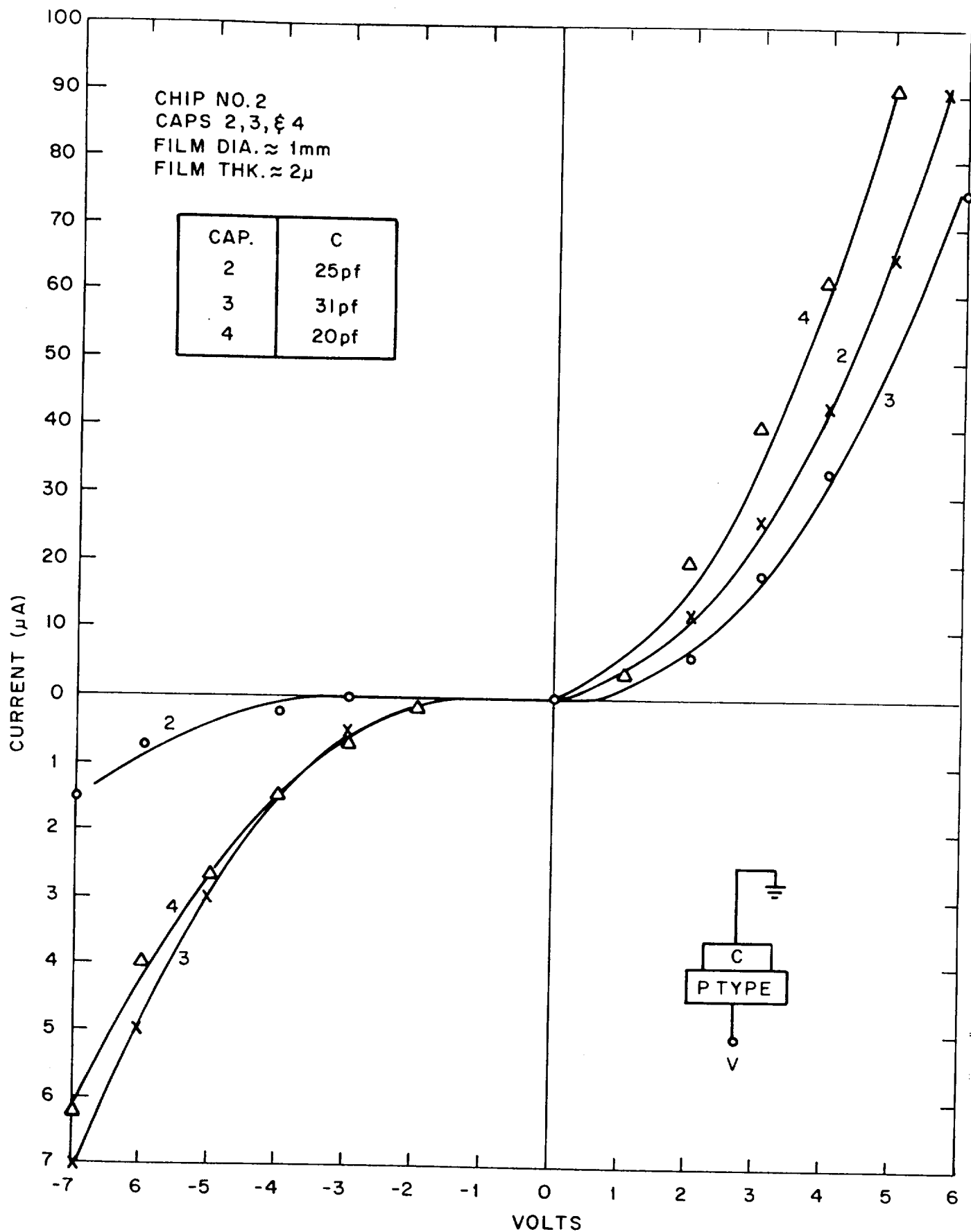


FIGURE 20.  
CURRENT-VOLTAGE CHARACTERISTICS.

features make it apparent that the diode characteristic is inherent to the carbon-silicon interface and not an accident associated for instance with the capacitor contact. First, when the substrate material is changed from N to P type, the polarity of the diode reverses. This can be seen by comparing the polarities indicated in Figs. 19 and 20. Second, to insure that no unexpected effects were coming into play, contacts were made to a bare silicon substrate and the current-voltage characteristics of this configuration were measured. No diode properties were observed as can be seen by reference to Fig. 21. The conclusion is that a diode junction exists at the carbon-silicon interface and is probably a partial result of impurity charge at the interface. It will be remembered that the existence of such charge was predicted by the observed translation of the capacitance-voltage characteristics mentioned earlier.

The characteristics shown in Figs. 18, 19 and 20 fit the model of a series combination of a resistor and diode, where the resistance is that of the bulk carbon and the diode results from the above-mentioned effect at the carbon-silicon interface. The general level of leakage current is fairly high, typically in the microamp region, and this is unexpected for a good carbon film. The apparent explanation is the existence of pinholes or partial pinholes or grain boundaries which provide low resistance leakage paths through to the substrate. Thus the resistance is fairly low and the diode characteristic prevails.

It was possible, however, to also fabricate capacitors which exhibited very low leakage and no diode nature. By using a more defect-free carbon film of about 2 microns thickness, a leakage characteristic similar to that shown in Fig. 22 resulted. Here the resistance of the bulk carbon is high and any diode effects are swamped out by the series resistance. Leakage currents of roughly 300 pA at  $\pm 5$ v are the result.

5.4.5 Stability--An accelerated test for stability with time and temperature was performed on two capacitors and preliminary results are encouraging.

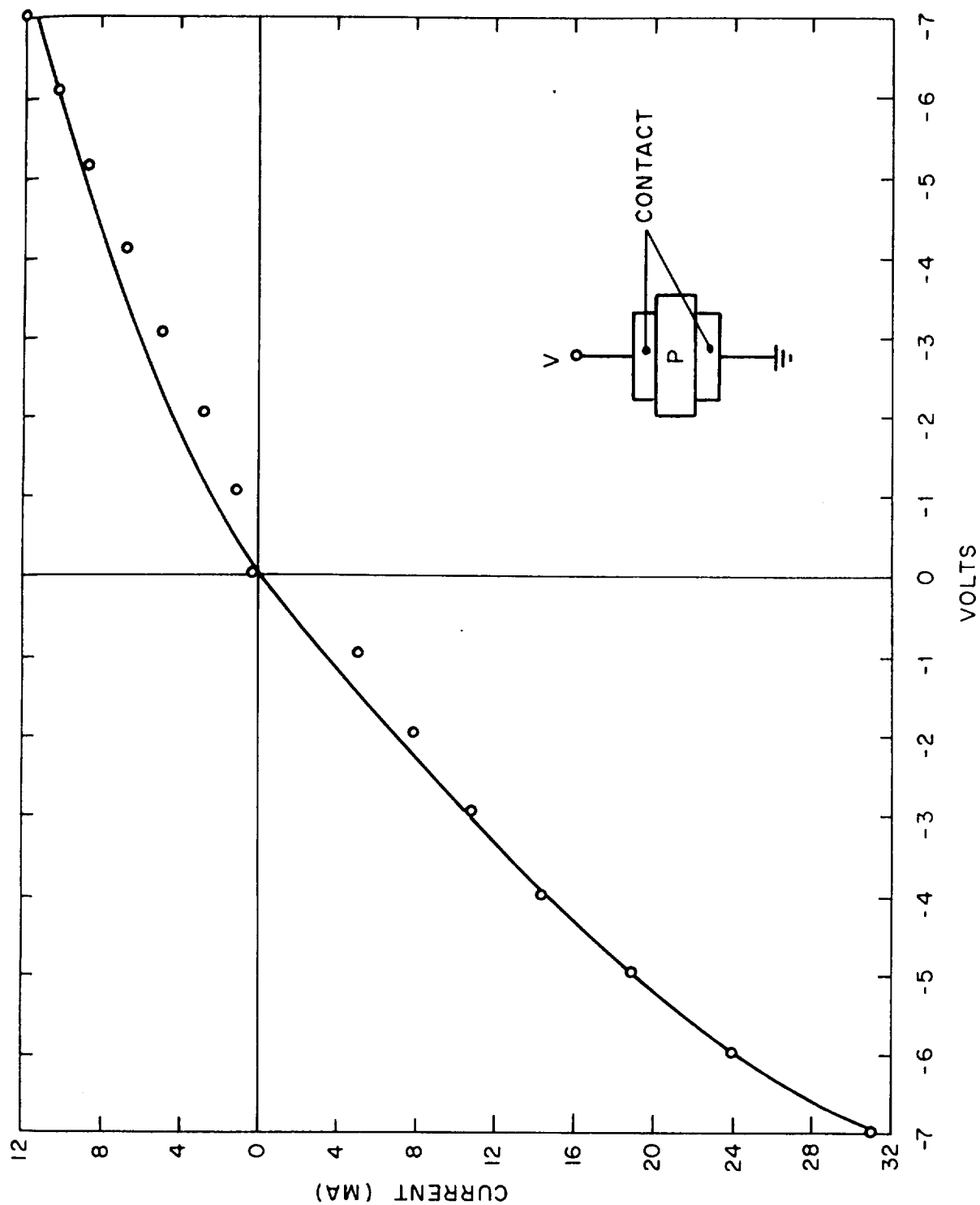


FIGURE 21.  
CONTACTS TO P-TYPE SILICON (BARE SUBSTRATE)

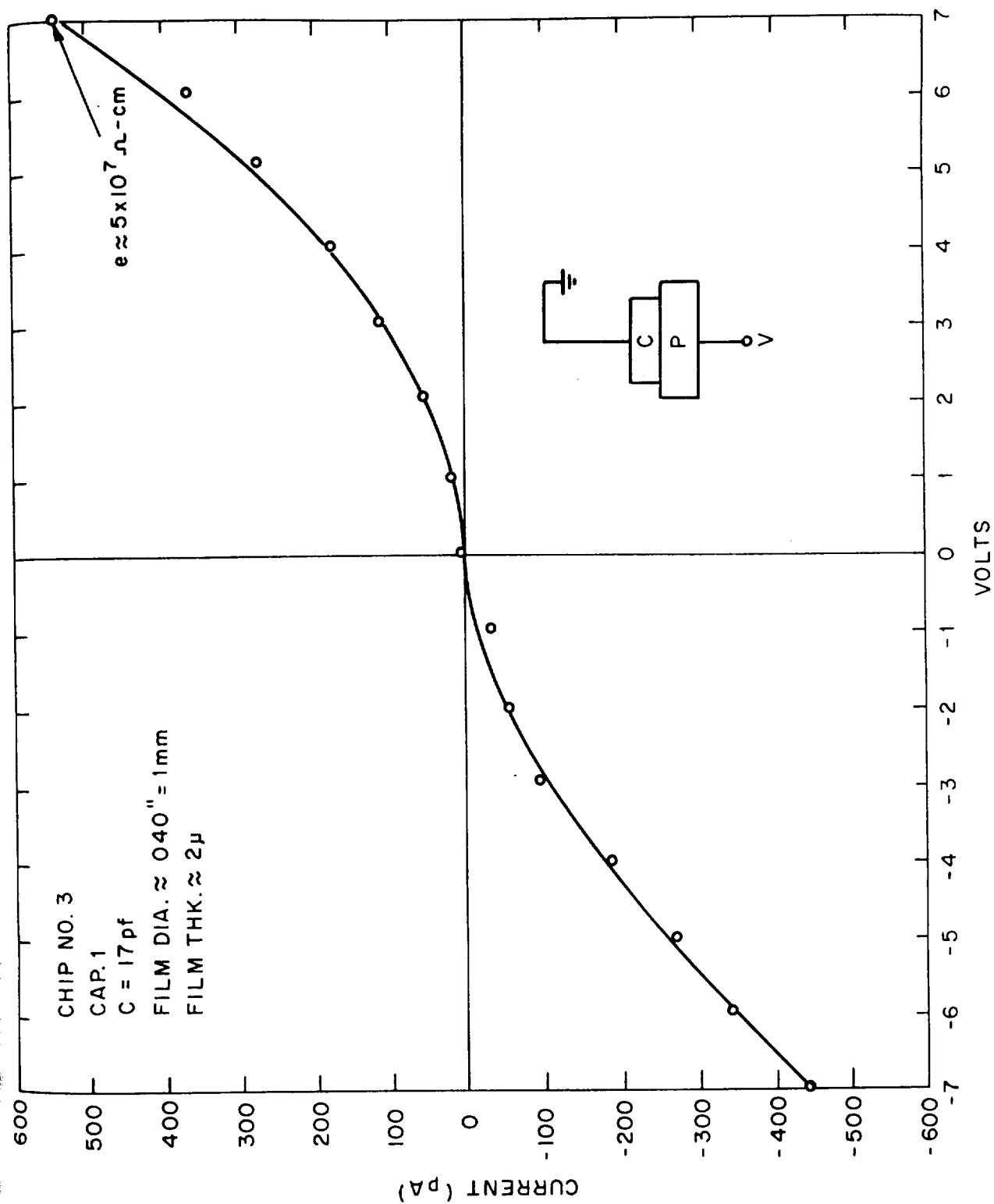


FIGURE 22 . CURRENT-VOLTAGE CHARACTERISTICS.

A common problem, particularly with MOS devices, arises from the drift or diffusion of ionic charge through the oxide layer at high temperatures. The result of this is a shifting of the capacitance-voltage characteristics of the device<sup>3</sup>. Fig. 23 illustrates this effect reported for the gate junction of a MOS FET<sup>3</sup>.

Because of the small radius of the carbon atoms used in fabricating the capacitors, a resistance to diffusion of ionic charge was expected. To investigate this, the following test was performed. The capacitance-voltage characteristics of two capacitors were measured before and after annealing at 127°C for 30 minutes. Next, the capacitors were rinsed in a 20% solution of NaCl and then flushed with distilled water. They were next subjected to a temperature of 127°C for 30 minutes under 4 volts bias and the capacitance-voltage characteristics were again measured after the device returned to room temperature. The resulting curves are plotted in Figs. 24 and 25.

In both cases, initial heating of the capacitor resulted in a displacement of the original curve apparently due to rearrangement of impurity distributions within the device<sup>\*</sup>. But after this initial annealing process (probably due to diffusion of sodium impurities built into the film during deposition), the capacitance-voltage curve changed very little. That is, there was very little evidence of diffusion of sodium ions through the carbon. This was particularly true of capacitor #3 in Fig. 24, where the curves before and after the sodium contamination are almost identical. Fig. 25 is perhaps not as completely convincing, but considering the severity of the test, the observed drift is not substantial.

Reference to Figs. 24 and 25 also shows a sharp decrease in capacitance around -5 to -8 volts indicating breakdown of the device at this point. A plot of current versus voltage as shown by the dotted curve in Fig. 24 confirms that breakdown is indeed occurring here. This was expected considering

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<sup>\*</sup> This phenomenon was also observed by Dr. E. Apgar and is apparent in Figs. 13 and 17 presented earlier.

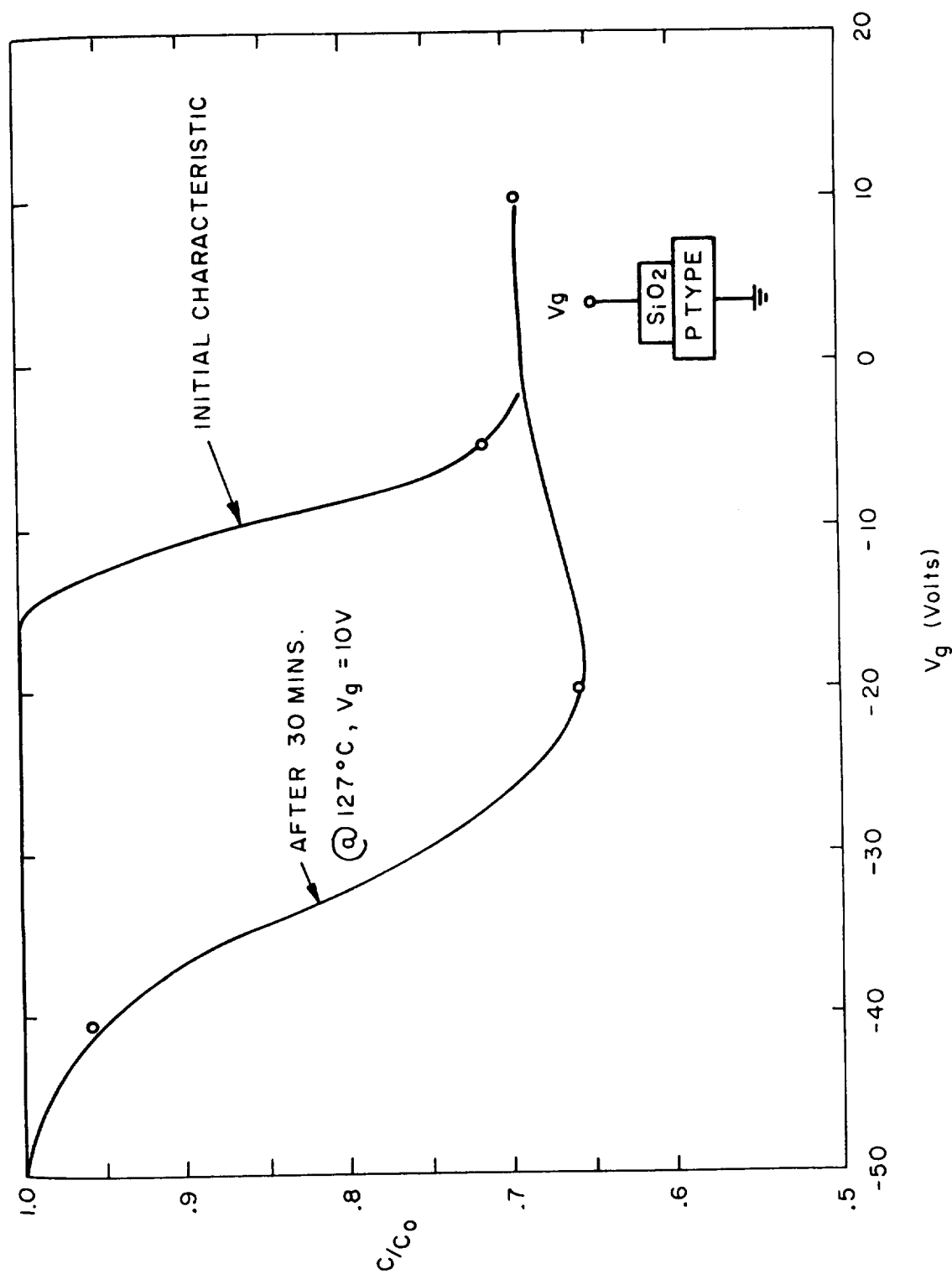
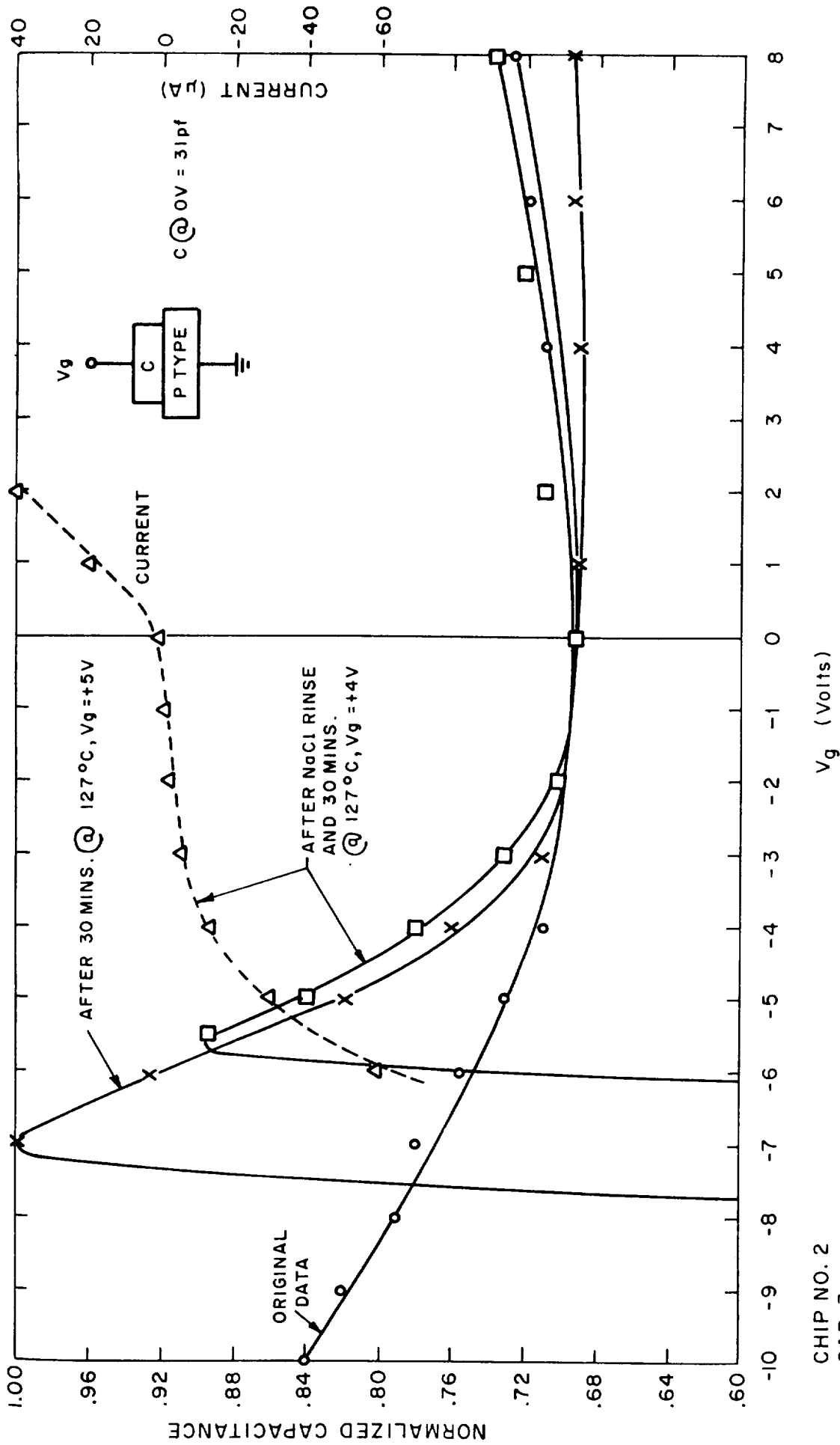


FIGURE 23 .  
 SHIFT IN CAPACITANCE - VOLTAGE CHARACTERISTICS DUE TO  
 IONIC CONTAMINATION FOR MOS DEVICE.\*  
 \*FROM REF 3



CHIP NO. 2  
CAP. 3

FIGURE 24.  
 $Na^+$  ION DIFFUSION TEST.

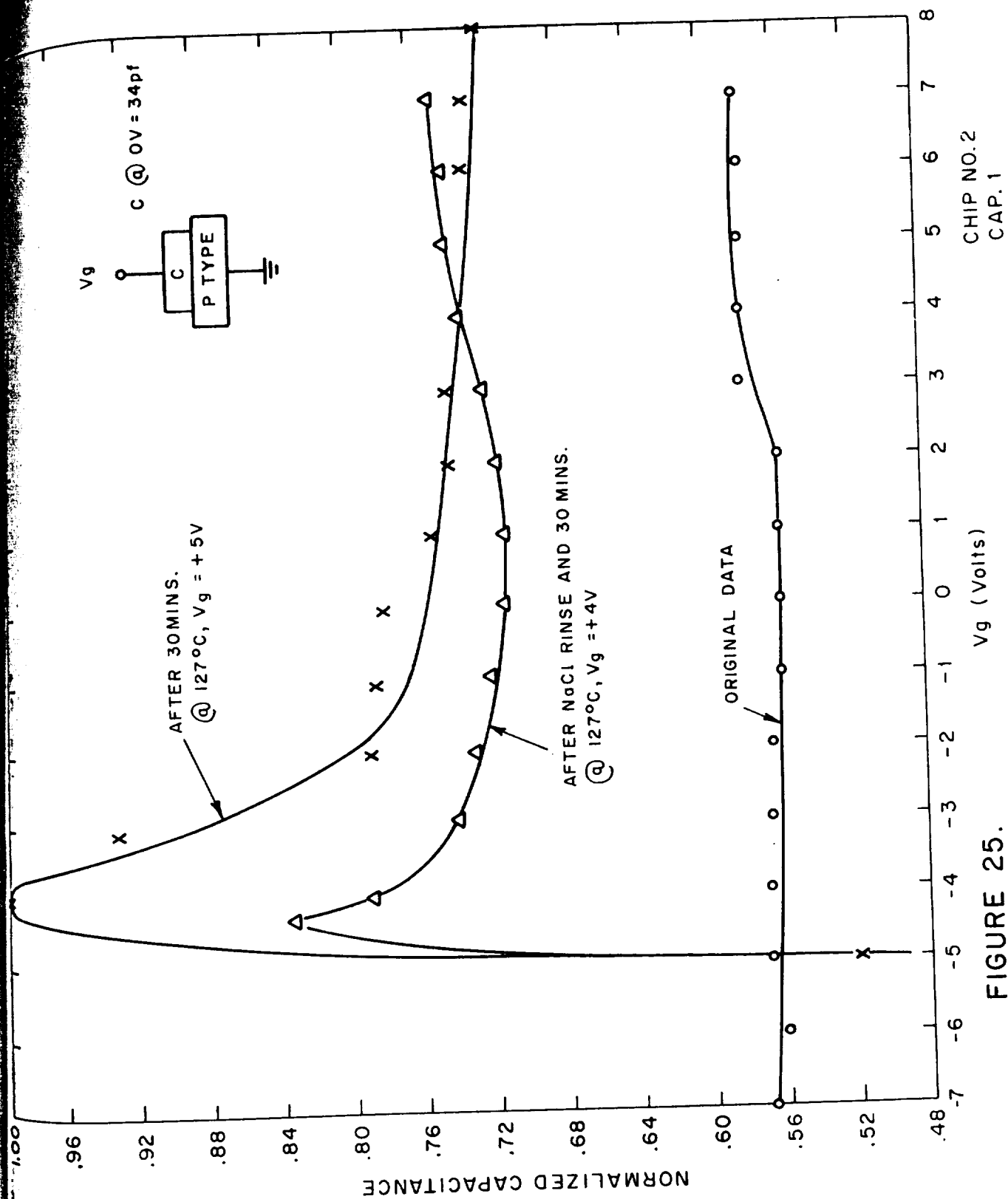


FIGURE 25.  
Na<sup>+</sup> ION DIFFUSION TEST.

that the capacitor here considered (Cap. #3 from Chip #2) was one which was initially found to have a predominantly diode-like current-voltage characteristic (see Fig. 20). For capacitors where the resistance of the carbon film swamps out the effect of any diode at the carbon-silicon interface (such as that shown in Fig. 22), this breakdown should occur at higher voltages.

5.4.6 Radiation Resistance--Considering the properties of the insulating carbon, it is expected that radiation-ionizable traps should be very few in number. That is, the carbon layer should be radiation resistant. If we accept a popular model, radiation induced charge occurs via the following simplified steps: electron-hole pairs are generated in the insulator by irradiation; defect sites in the insulator trap either an electron or hole, thus leaving an excess of the opposite charge to drift to one surface.

For radiation resistance, the carbon film immediately has a two-fold advantage over such materials as silicon oxide. First, its apparently very high band-gap makes the radiation induced generation of electron-hole pairs very difficult. Second, even if electron-hole pairs are generated, there should be very few defect sites in the tightly bound diamond-like structure to function as trapping centers.

Preliminary tests to investigate the radiation-resistance of the carbon films have been performed and are encouraging. Briefly, the results show no significant shift in the C-V characteristics and no increase in leakage for unbiased devices subjected to  $10^6$  rads from a cobalt-60 source.\* For devices subjected to the same radiation dosage under an applied bias, definitive results have not yet been obtained, probably because of the bonding difficulties encountered with transportation of samples with spring loaded contacts to the irradiation facility.

A total of six carbon film capacitors were tested. Two of these were to be irradiated under bias, and spring loaded probe contacts were used to make the required electrical contact to these two devices. However, prior

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\* Irradiation performed through cooperation of AFCRL, Hanscom Field, Bedford, Massachusetts.

to irradiation, leakage current on these devices increased from 5 nano-amps to several micro-amps at +5v, this apparently due either to movement of the probe contacts and scratching of the aluminization and film, or to the effect of voltage breakdown under DC bias which was applied prior to irradiation. One of these devices was eliminated from the test. The other showed no increase in leakage and no shift in flat band voltage after exposure to  $10^6$  rads under +5v bias. It must be noted, however, that the lack of a shift in the C-V characteristic here is not necessarily confirmation of radiation resistance, since it is possible that any radiation induced carriers could have been discharged through the leaky device ( $\sim 2\mu\text{a}$  at +5v).

For the case of unbiased devices, results were much more conclusive. Four such devices were tested. Leakage current both before and after irradiation was low, generally about 10 na at  $\pm 5$  v, and still no significant shift in C-V characteristics occurred; the largest shift was 0.5 volt after irradiation.

Results from these preliminary tests, then, are encouraging. Further radiation testing of low leakage devices under bias and with better bonding of the leads is necessary to definitely establish the radiation resistance of the carbon films.

5.4.7 Summary and Conclusions--A number of thin film capacitors using a diamond-like carbon film as the dielectric have been fabricated on silicon substrates. Capacitances of 25 pf are typical for film thicknesses of  $3\mu\pm 50\%$ ; and very low leakage currents are possible when care is taken to avoid pinholes in the dielectric. Both polarized and non-polarized devices were constructed; the former effect seems to result from defects in the carbon film which lower the resistance of that film and thereby permit dominance of the current-voltage characteristics by the diode at the carbon-silicon interface. Non-polarized devices resulted when more defect-free films were used. These were characterized by a high bulk carbon resistance and had leakage currents in the  $10^{-12}$  amp region. Preliminary measurements indicate a resistance to sodium ion diffusion and this bodes well for the stability of the devices. Other points of interest relevant to the devices made are as follows:

(a) Correlation between theoretical and experimental values of capacitance indicate a high dielectric constant,  $k$ , near that of diamond, for the carbon film, although there is some difficulty in reproducibly depositing such films. Since capacitance per unit area ( $C/A$ ) varies as  $k/d$ , where  $d$  = film thickness, high values of  $C/A$  should be possible when very thin films are used. For instance, for a film thickness of  $1000\text{\AA}$ , capacitance per unit area should be about  $1.0\text{ pf/mil}^2$ .

(b) High radiation resistance is associated with high energy gap materials.<sup>5</sup> Since diamond is characterized by a gap width of 5.3 volts (as compared to 1.1 volts for silicon) devices fabricated from such a film should be radiation resistant. Limited radiation resistance measurements appear to support this expectation.

(c) The density of surface states at the carbon-silicon interface is calculated to be about  $5 \times 10^{11}\text{ cm}^{-2}$ .

## 5.5 Thin Film Transistors

5.5.1 Introduction--Most of the work in fabricating carbon thin film capacitors was performed as the first step toward FET, or more properly thin film transistor (TFT), construction. The fabrication of TFT's using stencil masks and ion beam deposition on room temperature substrates is described in what follows.

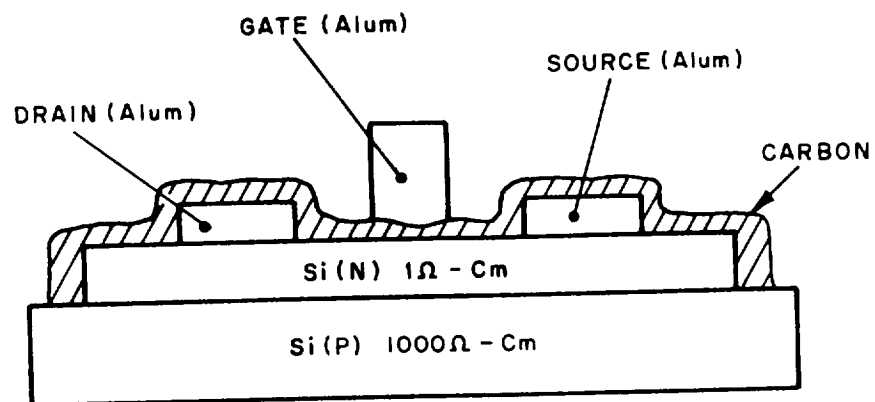
5.5.2 Geometry--Two types of thin film transistors (TFT's) have been made, one type having a coplanar configuration and one with an inverted coplanar structure. These geometries are shown in Fig. 26. For each device the following approximate dimensions apply:

Thickness of deposited silicon-- $5000\text{\AA}$

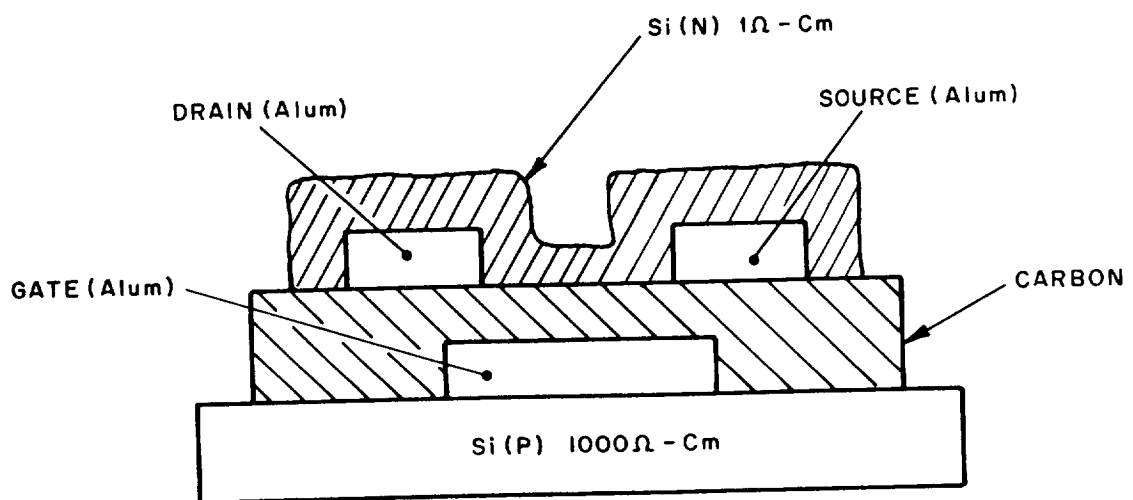
Thickness of deposited carbon-- $1000\text{\AA}$

Channel width = drain source separation -  $0.5\text{ mil}$

As mentioned earlier, stencil masks were used in the fabrication of these devices. Fig. 27 illustrates the mask used. The mask was so designed that alignment for each successive deposition was achieved by rotating the mask  $90^\circ$  and using the indexing markers a, b, c, d to position the mask properly. Alignment was done manually.



COPLANAR



INVERTED COPLANAR

FIGURE 26  
FET GEOMETRIES.

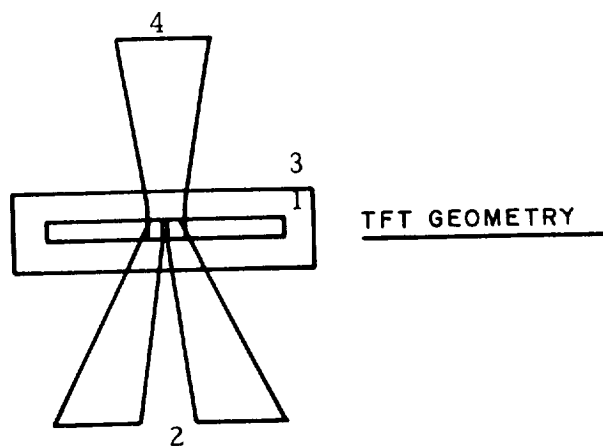
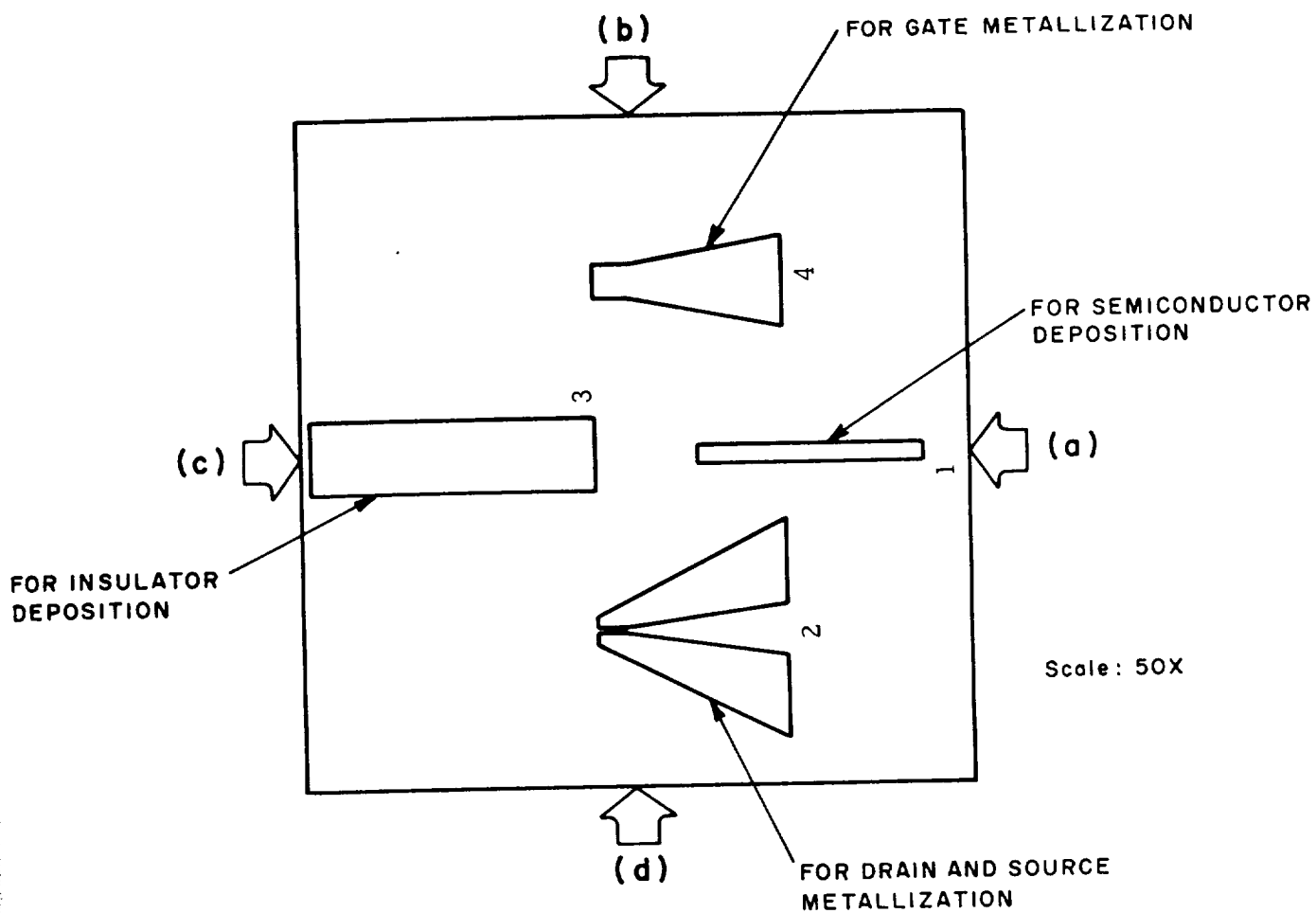


FIGURE 27 .  
STENCIL MASK FOR TFT FABRICATION.

5.5.3 Characteristics of a Coplanar TFT--The current-voltage characteristics of a coplanar TFT as measured with a Tektronix 576 Curve Tracer are shown in Fig. 28. As can be seen by reference to Fig. 26, the devices built were intended to operate as N-channel TFT's; that is, for a given drain-source voltage ( $V_{DS}$ ), drain current ( $I_D$ ) should decrease as the gate voltage ( $V_G$ ) is decreased.

This effect does indeed occur in Fig. 28: drain current is maximum at  $V_G = 0V$  and decreases as  $V_G$  becomes more negative. Operation of this device at first appears to be in the depletion mode, but a closer look at voltage polarities indicates that the device is actually operating in the enhancement mode. This can be seen by observing that the drain-source voltage ( $V_{DS}$ ) in Fig. 28 is negative; in other words the terminal originally designated as the drain is actually functioning as the source. Accordingly gate voltage ( $V_{GS}$ ) must be re-referenced to the terminal originally called the drain if the usual polarity conventions are to be observed. If this is done, it can be seen that drain current is low at 0 gate voltage and increases as gate voltage increases; that is, the device functions in the enhancement mode. There are several difficulties, however, first the transconductance of the device as measured from the characteristic curves is very low, about 1 micromho. Also the voltage amplification factor is low, close to 1. Finally, channel resistance is extremely high, about 1 megohm. If the anticipated channel resistance is calculated from the dimensions of the channel and the resistivity of the deposited silicon, one gets about  $2K\Omega$ :

$$R = \frac{\rho \ell}{A} = 2K\Omega$$

$$\rho = 1\Omega\text{-cm}$$

$$\ell = 2 \times 10^{-3} \text{ cm}$$

$$A = 10^{-6} \text{ cm}^2$$

It is theorized that the phenomenon responsible for these difficulties is quite possibly the formation of a thin layer of silicon oxide between the low resistivity silicon and the drain and source aluminum contacts during fabrication.

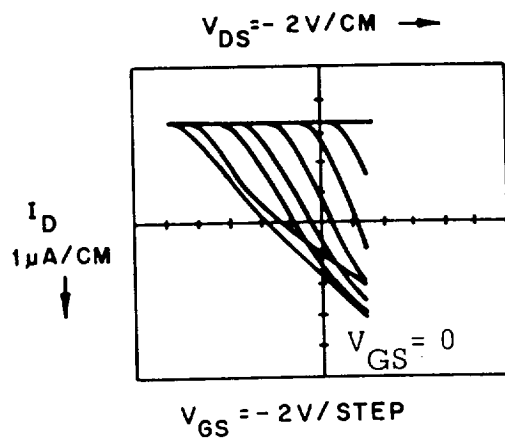


FIGURE 28  
COPLANAR TFT.

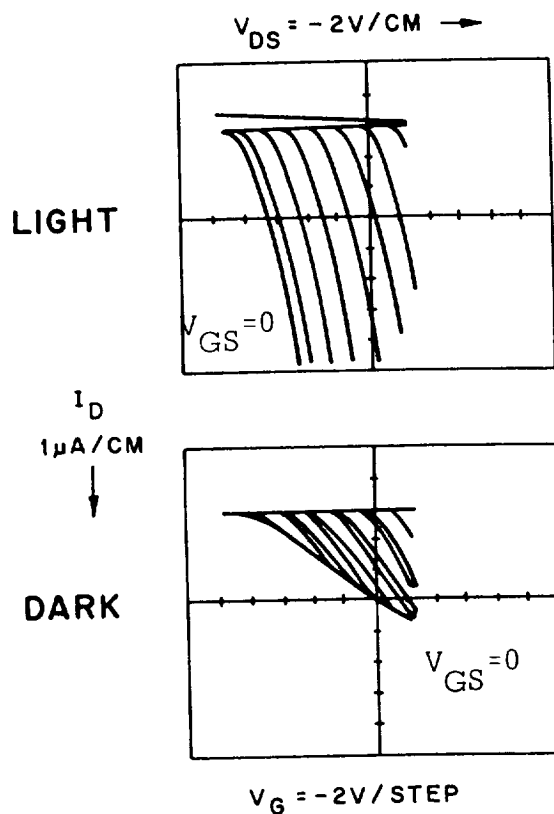


FIGURE 29  
LIGHT SENSITIVITY  
OF COPLANAR TFT.

This would explain the high resistance between drain and source and the low transconductance. The result of this is that drain-source signal current is reduced to the level of leakage currents in the device--of the order of microamps--and only degenerate FET characteristics are obtained. The system was let up to atmospheric pressure during each step involving manual rotation of the stencil mask. This could explain the appearance of insulating films for the drain and source contacts.

An interesting observation made in the course of this work was that the device described above, and indeed other devices subsequently built, showed a strong sensitivity to light. This is demonstrated in Fig. 29 which shows the I-V characteristics for the device under normal lab lighting and then under increased illumination with a low-intensity lamp. It is to be noted that the effect of increased illumination is to cause an increase in transconductance of the device and not merely a shunt path between source and drain. Similar observations have been made by others, particularly with cadmium sulfide TFT's. Fig. 30 shows such a cadmium sulfide unit reported to exhibit very strong sensitivity to light.<sup>11</sup>

5.5.4 Characteristics of Inverted Coplanar TFT--In order to eliminate the possibility of silicon oxide formation between the silicon layer and the aluminum contacts, it was decided to fabricate an inverted coplanar TFT. As can be seen by reference to Fig. 26 this geometry requires the silicon layer to be the last deposition made; consequently, any oxide formation over this layer has the beneficial effect of passivating the surface rather than interfering with device operation as in the normal coplanar case. Indeed better results were obtained for this configuration.

The drain-source characteristics for an inverted coplanar TFT are shown in Fig. 31. As before, the device is an N-type enhancement mode TFT; the same voltage polarity considerations mentioned earlier should be applied. From these characteristic curves the following parameters have been measured:

$$\text{Transconductance} = g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \bigg|_{V_D = 14V} = 75 \text{ micromho}$$

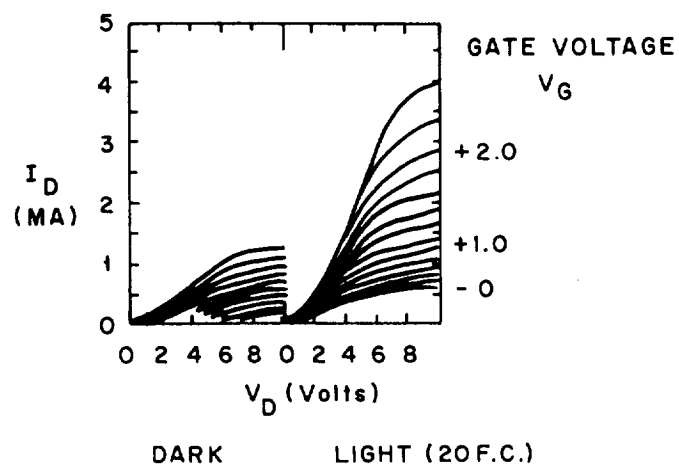


FIGURE 30

Operating characteristics of a photosensitive cadmium sulfide TFT\*

\*Ref. 5 --Weimer, "Insulated Gate Thin Film Transistor", Physics of Thin Films, Vol 2.

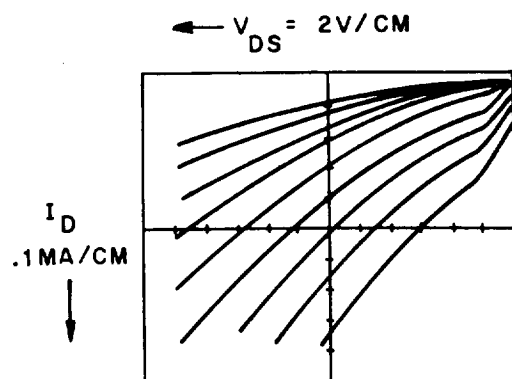


FIGURE 31.  
INVERTED COPLANAR TFT.

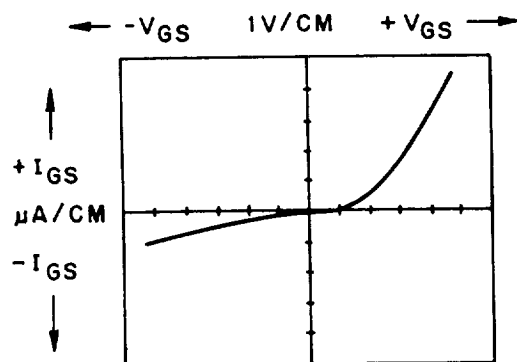


FIGURE 32 .  
GATE CHARACTERISTICS OF  
INVERTED COPLANAR TFT.

$$\text{Output impedance} = R_0 = \left. \frac{\Delta V_{DS}}{\Delta I_D} \right|_{V_{GS} = 8\text{v}} = 22\text{K}\Omega$$

$$\text{Voltage amplification factor} = \mu = \left. \frac{\Delta V_{DS}}{\Delta V_{GS}} \right|_{I_D = 0.5 \text{ ma}} = g_m R_0 = 1.7$$

The gate characteristics of this device were also measured and are shown in Fig. 32. These measurements were made with drain and source shorted to ground. The input impedance as measured from these curves is about 60K $\Omega$ .

It is apparent from this data that an active device, a thin film transistor with an amplification factor greater than unity has been made. It is equally apparent that device quality requires considerable improvement. This latter fact was indeed anticipated considering the details of the fabrication process; e.g. manual alignment of stencil masks for each stage of deposition. However, the goal of this research has been first to demonstrate the feasibility of TFT construction; the most direct means within the limits of time and funds available for the program were taken to that end. The fabrication of additional devices and improvement of device quality are the logical next steps. Consideration of some of the problems with the TFT's thus far deposited is in order.

Reference to the data presented above for the inverted coplanar structure indicates that the transconductance (75 micromho), the output impedance (22K $\Omega$ ) and the input impedance (60K $\Omega$ ) are all undesirably low. The major causes of these difficulties seem to stem from the following facts. First, manual alignment of the stencil mask is a difficult task. As the TFT's were made, microscope photographs were taken to examine how accurately mask alignment had been achieved; in most cases the devices which performed most poorly were those which had relatively poor mask alignment. Second, the alignment task was performed out of the vacuum system, thereby exposing the devices to possible contamination. Third, film thickness was not extremely well controlled; some of the leakage problems encountered probably resulted from pinhole defects

in films that were too thin. Finally, control of film purity in the deposition system is a task that requires constant attention and represents a possible source of problems.

A number of other observations on device performance also merit description. For instance, as can be seen from the characteristic curves presented earlier, the devices in general do not saturate. Weimer<sup>11</sup> has reported a number of effects which can lead to this behavior. Among these are (1) an unmodulated parallel conductance path between source and drain, (2) insufficient electrostatic shielding of the gap region from the drain field by the gate, (3) internal breakdown in the semiconductor channel, and (4) insulator breakdown. Also observed for some devices, such as Fig. 28, were hysteresis loops in the device characteristics. There are, again, a number of possible causes for this, including the existence of slow states, and effects such as internal heating, capacitance or inductive transients.<sup>11</sup> Another possible cause of such loops can be the existence of a nonhomogeneous stratified insulator layer having a dielectric relaxation time near the gate which differs from that near the semiconductor.<sup>11</sup> A final fact to be noted is that although detailed stability tests were not made, the characteristics of devices built generally showed no marked deterioration over periods of at least a week.

## 6 GENERAL SUMMARY

The following is a summary of the more important results of work performed in this program.

- (1) An ion beam deposition system capable of depositing thin films on room temperature substrates has been designed and constructed. By appropriate control over deposition parameters, semiconducting, metallic, and dielectric films have been deposited.
- (2) Single crystal silicon films have been deposited on room temperature silicon substrates. Silicon films have also been deposited on glass.
- (3) It has been possible to deposit molybdenum films on silicon substrates.
- (4) The deposition of dielectric films such as  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , and insulating carbon was tried. The relatively greater success in depositing an insulating carbon film with a number of diamond-like properties led to exploitation of this film as an insulator for thin film devices.
- (5) A study of the properties of silicon films on silicon substrates was performed. Thermal emf measurements indicated that both N and P type films were deposited on both N and P type substrates. Study of film rectification characteristics showed that the silicon film-silicon substrate junction has a diode nature.
- (6) A multi-ion beam source for depositing metal-insulator-semiconductor devices was designed; in particular, insulating carbon, semiconducting silicon, and aluminum were the deposition materials involved.
- (7) Thin film capacitors using insulating carbon as the dielectric were made. Results included the following information: capacitances were roughly  $0.02 \text{ pf/mil}^2$ ; leakage currents in the pico amp range were attained; voltage breakdown up to  $\pm 40\text{v}$  was observed; surface state density was of the order of  $10^{11} \text{ cm}^{-2}$ ; a resistance to sodium ion contamination was observed; adherence of carbon dielectric to silicon substrate was about  $2000 \text{ gm/cm}^2$ . This work was intended primarily to lay the foundation for TFT fabrication; that is, capacitors were not the final goal. Accordingly, effort was directed to obtaining functional, not optimized, devices.

(8) Thin film transistors using ion beam deposited silicon and carbon, and evaporated aluminum contacts were made. A coplanar and an inverted coplanar geometry were tried. The latter geometry was the more successful of the two yielding, as with the capacitors, a device that was functional while not intended to be optimized. This was accomplished using manually aligned stencil masks through which films were ion beam deposited on room temperature substrates.

(9) Radiation resistance was demonstrated for insulating carbon capacitors.

## 7 ACKNOWLEDGMENT

The assistance of James B. Dodge, Rodney A. Hopkins, and Robert Kleiman is gratefully acknowledged. The interest and encouragement as well as the technical assistance of Dr. E. Apgar has been of considerable value.

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## APPENDIX A

### Electron Diffraction Measurements

By the use of the deposition system that has been described, it has been possible to grow films of single crystal silicon on single crystal silicon substrates. The evaluation of the film crystal structure was made by electron reflection diffraction analysis performed by Manlabs, Inc., Cambridge, Mass. Silicon film deposits were formed on a number of single crystal substrates with a (111) orientation. Five of the films were sent out for low energy electron diffraction measurement. The specimens were sectioned to provide small specimens containing the deposit area. These specimens were analyzed by reflection electron diffraction procedures using a Hitachi HU 11 electron microscope operated at 100 kV ( $\lambda_E = 0.04 \text{ \AA}$ ). The electron beam was at a grazing angle of incidence of about  $1^\circ$  relative to the specimen surface. Electron diffraction through reflection from the surface was studied; for this case the diffraction is estimated to be limited to about the first 10 to  $20 \text{ \AA}$  in depth from the surface.<sup>17</sup> The effective depth of penetration can be considerably deeper if the surface is roughened or can be lower, if the electron voltage is reduced. The beam was used to scan the deposit to show that the film was uniform.

### Electron Penetration Depth

A study was made of the electron penetration depth for the interpretation of the electron diffraction measurements of the films deposited on the thin film crystal substrates. It was desired to show that the penetration depth of the probing electrons was small compared to the film thickness so that the diffraction pattern is characteristic of the film and not of the substrate. It is estimated that the film thickness is about  $6,000 \text{ \AA}$ . A study was made of the probable penetration range of 100 kV electrons in silicon and it was found that the range was about  $1,000$  to  $2,000 \text{ \AA}$ . When one takes into account the fact that the electrons are arriving at a grazing angle of about  $1^\circ$ , the perpendicular penetration depth is reduced by a factor of  $\sin(1^\circ) = 0.0175$ , and the penetration depth is thus about 18 to  $36 \text{ \AA}$ .

The information about the electron diffraction range was difficult to obtain, but was finally located in a paper by Von Borries. He considered the situation for a number of materials<sup>10, 18</sup>. Von Borries studied the problem of the visibility of the electron diffraction pattern and the penetration or probing distance of the electron beam. He was able to define the transmitting thickness  $\Delta$  (mass thickness density) as the thickness which on the average elastically scatters each electron once during its passage. For thicknesses greater than  $1.5\Delta$ , the contrast is so flat that no details can be discerned. Taking into account inelastic scattering also, he shows that this thickness corresponds closely to that value which still gives a clear electron image necessary for identification of details. This characteristic thickness is relatively independent of the nature of the material. Table A-1 shows the characteristic thickness for various materials and for various beam energies. In regions where relativistic effects can be neglected, the characteristic thickness is proportional to the beam energy, but increases less rapidly above 100 kV. Practical experience shows good agreement with these estimates<sup>10</sup>. For compact films of metal, thickness not much above  $1,000\text{\AA}$  is the limit from the point of view of the necessary contrast in the resulting electron diffraction pattern.<sup>10</sup>

The conclusion to be drawn from the information that has been presented, is that the electron reflection diffraction measurements (at  $1^\circ$  grazing angle) are characteristic of the surface properties to a depth of approximately  $25\text{\AA}$ . Since the film thickness is greater than this measurement depth, (as is computed and as shown by the change of surface appearance) the reflection diffraction results at small grazing angles are not characteristic of the substrate but of the deposited film.

TABLE A-1

CHARACTERISTIC MAXIMUM TRANSMITTING THICKNESS FOR  
 CLEAR ELECTRON DIFFRACTION PATTERNS FOR<sup>(a)</sup>  
 VARIOUS MATERIALS AND ELECTRON ENERGIES

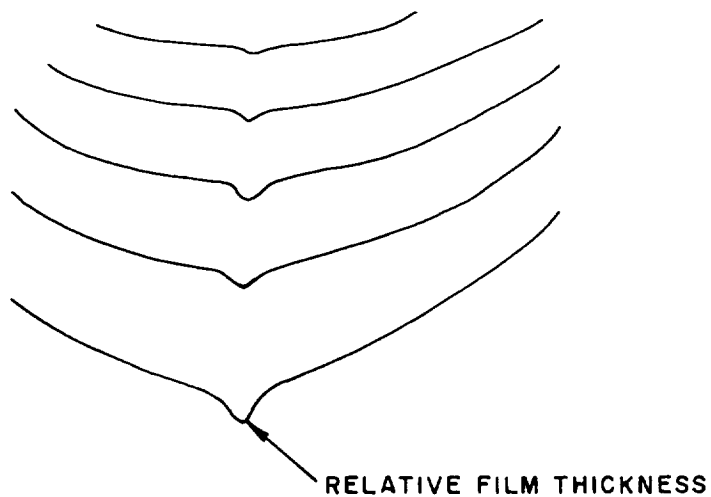
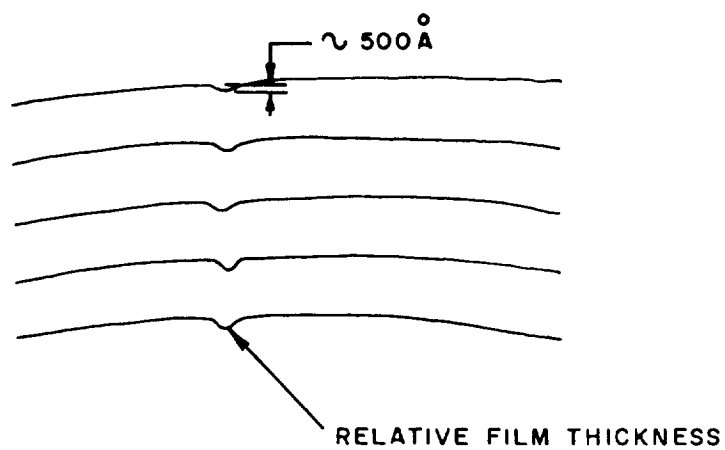
Element	Electron Energy		
	50 kV	100kV	500 kV
C	900Å	1600Å	4000Å
Al	----	1300Å	----
Cu	----	1050Å	----

---

(a) According to B. Von Borries, *Z. Naturforschag*, 4a, 52 (1949).

See also: V. E. Casslett, Practical Electron Microscopy  
 (Academic Press, London, 1951), p. 260.

## APPENDIX B



MEASUREMENTS OF CARBON FILM THICKNESS USING  
SLOAN ANGSTROMETER

## APPENDIX C

### Capacitance-Voltage Characteristics of Metal-Insulator-Semiconductor Structures

Consider first a device similar to the capacitors described earlier in this report, that is, a metal-insulator-P type silicon configuration. It will be recognized that this is the same configuration that might be used for the gate of an MOS FET. Assume for the present that there exists no contact potential nor work-function differences between the metal and semiconductor and that there are no charges at the carbon-silicon interface. Under these conditions the total capacitance of the structure is given by

$$C = \frac{1}{\frac{1}{C_c} + \frac{1}{C_s}} \quad (1)$$

where  $C_c$  is the bulk capacitance per unit area of the carbon film and  $C_s$  is the capacitance per unit area of the surface space charge region in the semiconductor. In other words, the total capacitance is the series combination of  $C_c$  and  $C_s$ . If a positive voltage  $V$  is now applied to the contact on the carbon film (this would be the gate in an FET), the semiconductor surface will begin to deplete and the capacitance is given by<sup>3</sup>

$$\frac{C}{C_c} = \frac{1}{\sqrt{1 + \frac{2k_c^2 \epsilon_0}{qN_A k_s L^2} V}} \quad * \quad (2)$$

where

- $k_c$  = dielectric constant of carbon film,
- $k_s$  = dielectric constant of semiconductor
- $N_A$  = impurity concentration, and
- $L$  = thickness of carbon film.

3

---

\*Reference 3 appears to contain a misprint in this equation. The corrected form is used here.

As  $V$  is increased, strong inversion occurs, at which point the depletion region will increase no more and the capacitance levels off. This effect is demonstrated in Fig. C-1 which shows the capacitance voltage characteristic of an ideal device.<sup>3</sup> Note also that for zero or negative voltages, the capacitance levels off and approaches that of the bulk carbon since no depletion region exists in these cases.

The voltage at which strong inversion sets in is of considerable importance in MOS FET's in that it is the "turn-on voltage" for the device. This point is indicated at  $V_T$  in Fig. C-1 and represents the point at which channel conductance for a MOS FET begins to increase.

Let us now remove the restrictive assumptions made at the start of this discussion and consider a real device. That is, consider what are the effects on device performance if there exists:

- (1) A difference in work functions between the metal and the semiconductor, and/or
- (2) impurity charge within the carbon layer.

It can be shown that either or both of these tend to cause a translation of the entire capacitance-voltage characteristic along the voltage axis. Fig. C-2 illustrates this phenomenon for the case of an MOS device.

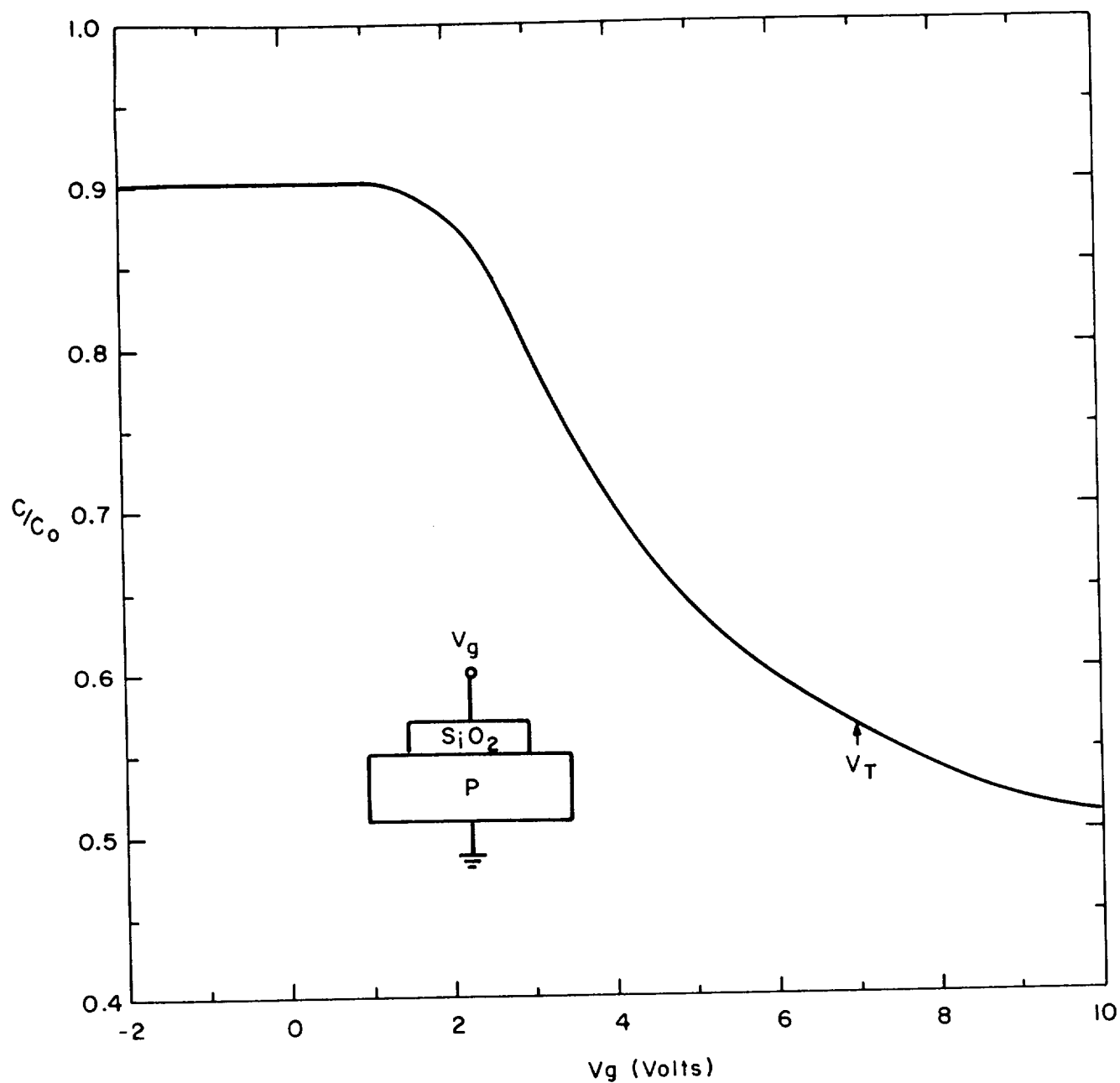


FIGURE C-1.  
CAPACITANCE VOLTAGE CHARACTERISTICS  
OF IDEAL MOS DEVICE.\*

\* From Grove, Physics and Technology of Semiconductor Devices(Ref. 3)

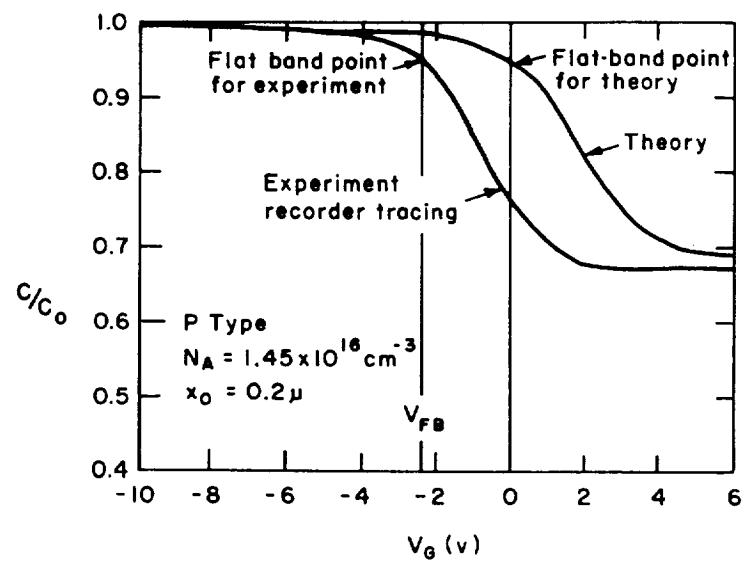


FIGURE C-2

The Combined Effects of Metal-Semiconductor Work Function Difference and Charges Within the Oxide on the Capacitance-Voltage Characteristics of MOS Structures \*

\* From Grove, Physics and Technology of Semiconductor Devices (Ref. 3)

APPENDIX D  
NEW TECHNOLOGY APPENDIX

During the course of this program in the following new technology items were devised:

1. "Low Energy Ion Beam Source for Deposition of Thin Films"

The innovation is described in pages 4 through 10.

This ion beam technique permits the use of an accelerating electric field to supply the energy necessary to make the deposited material mobile on the surface. The increased surface mobility of the deposited atoms permits them to nucleate into novel and thin film structures without the requirements of the usual high substrate temperatures.

2. "Diamond-Like Carbon Films"

Described in pages 22 through 54.

By means of the ion beam deposition source it was possible to deposit thin films of carbon in a form which is similar in many ways to that of diamond. In particular, the following features of similarity were observed: a) insulating, b) transparent, c) high index of refraction, d) dielectric constant similar to that of diamond, e) hard enough to scratch glass, f) resistant to hydrofluoric acid, and g) lattice structure, as determined by x-ray diffraction, similar to that of diamond. It was shown that these insulating carbon films are resistant to sodium ion diffusion and also appear to show a resistance to radiation in terms of stability of C-V characteristics and of leakage resistance.

3. "Active Device Fabricated Using Combination of Ion Beam Deposited Carbon and Silicon Films"

This technique is described in pages 54 through 63.

By using the ion beam deposition system together with both silicon and carbon sources, it was possible to deposit an active FET thin film device. Stencil masks were used. Current, gain, and light sensitivity were demonstrated.